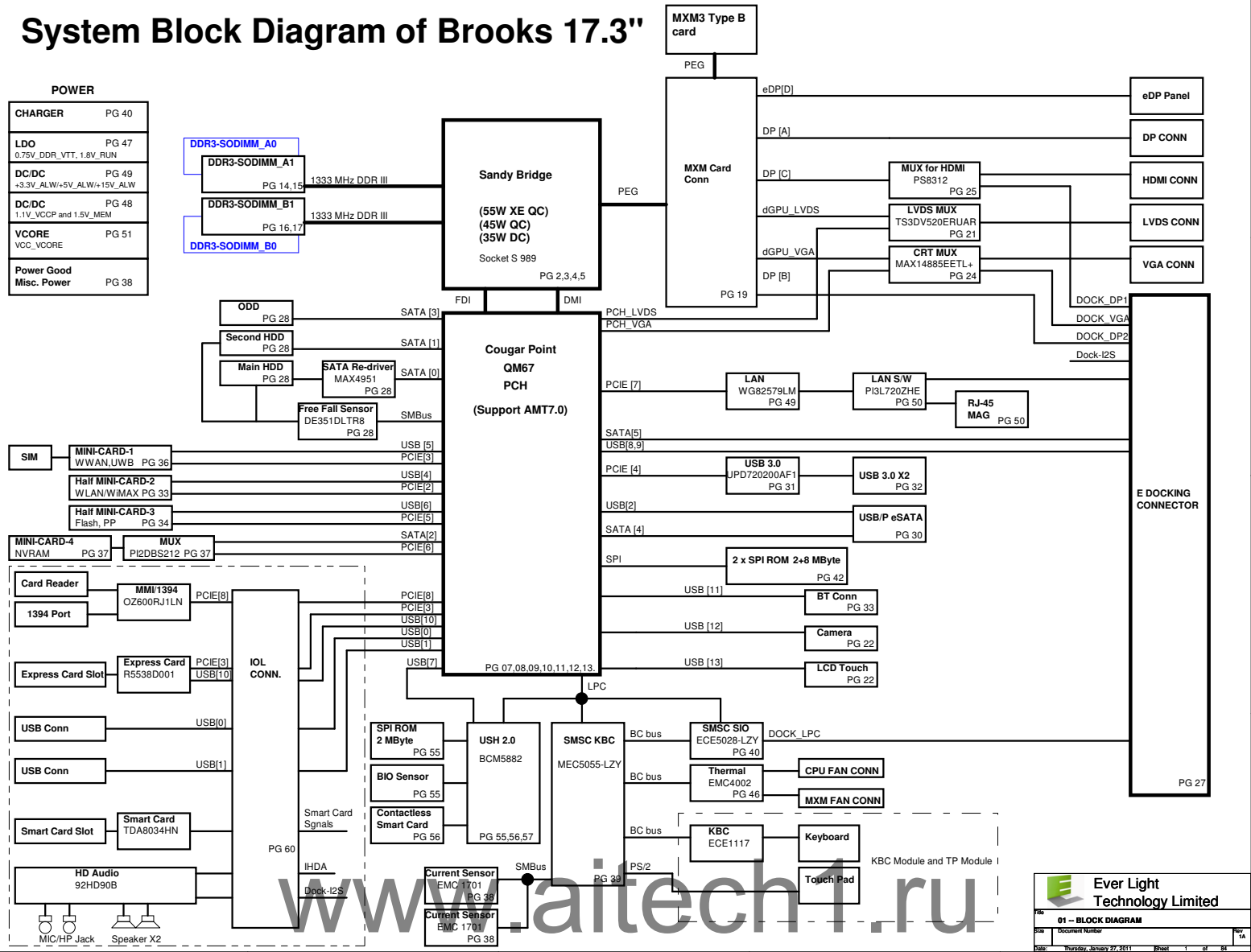
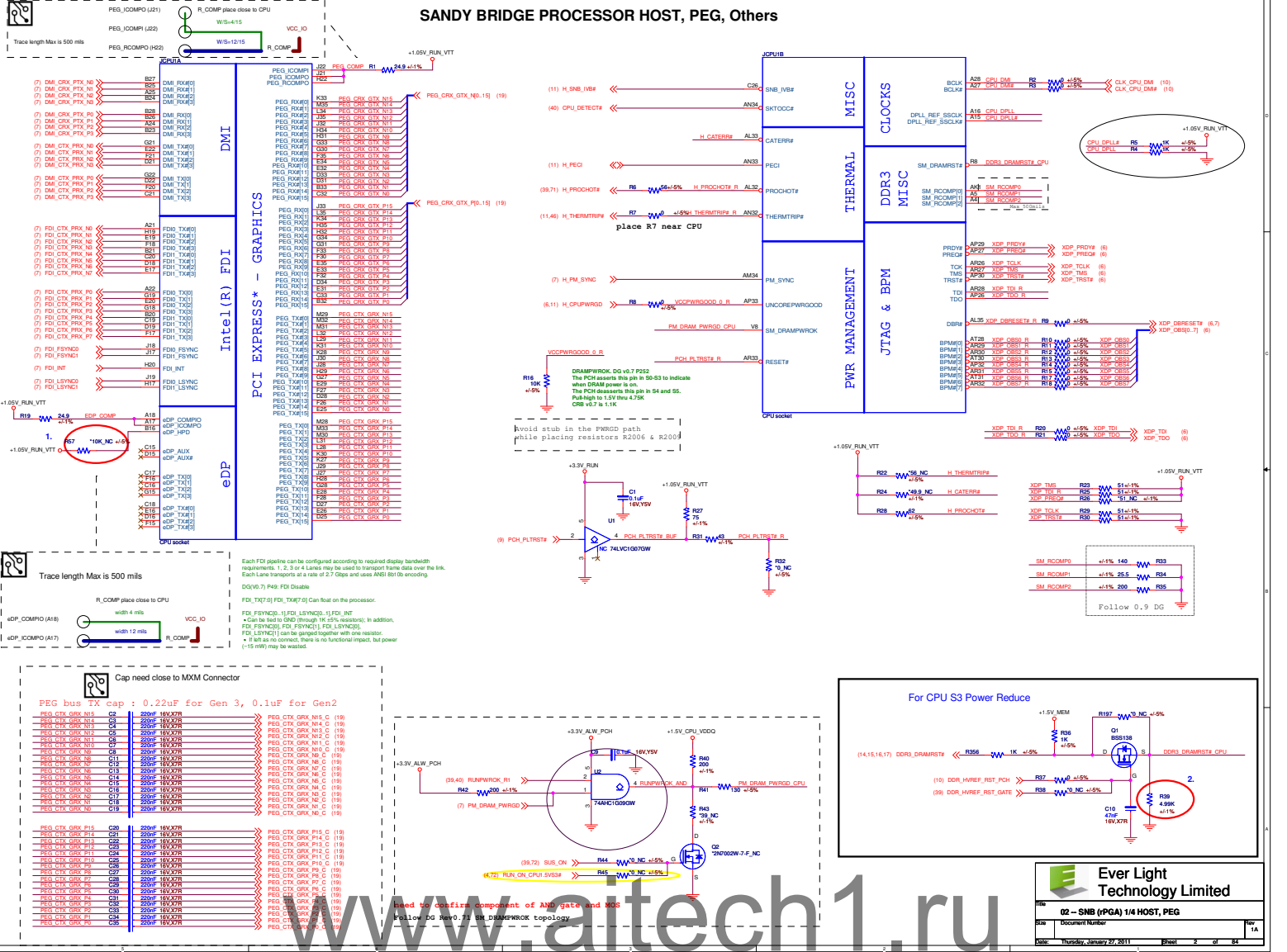
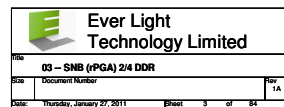


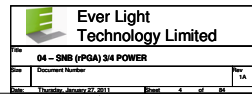
## System Block Diagram of Brooks 17.3"





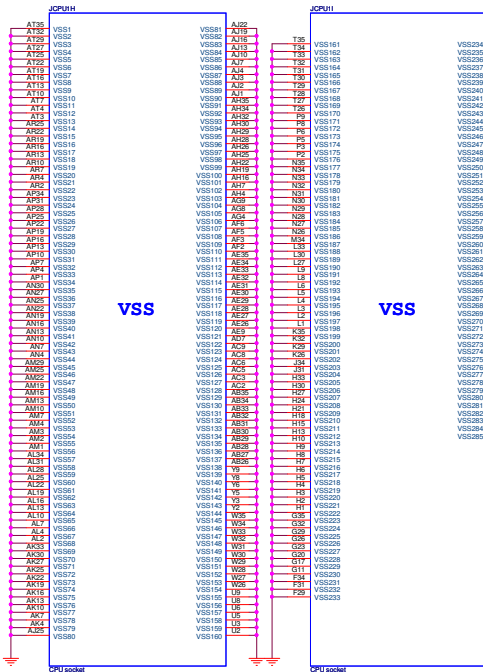
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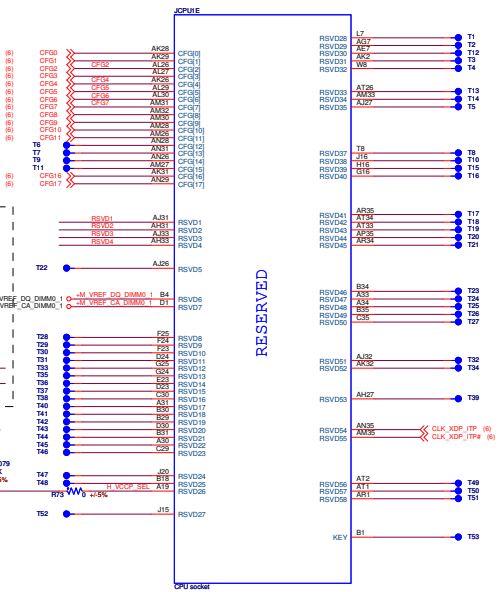




# SANDY BRIDGE PROCESSOR (GND)



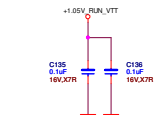
# SANDY BRIDGE PROCESSOR( RESERVED, CFG)



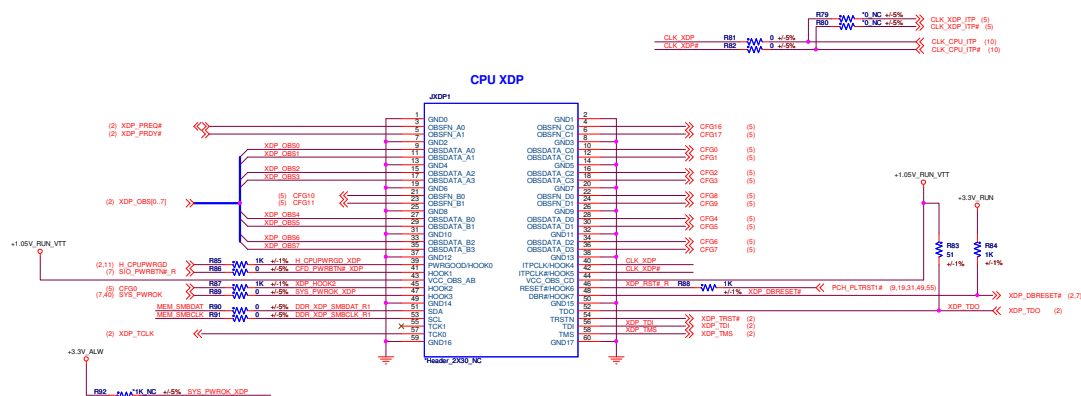
	1	0
CFG2 (PEG Static Lane Reversal)	Lan# definition matches socket pin map definition (Default Value)	Lan Reversed
CFG4 (Display Port Presence strap)	Disabled; No Physical Display Port attached to Embedded Display Port (Default Value)	Enabled; An external Display port device is connected to the Embedded Display port
CFG6-5		
CFG7 (PEG Defr Training)	PEG Train immediately following xxRESETB de assertion (Default Value)	PEG Wait for BIOS for training

CFG6-5 (PCIe Port Bifurcation Straps)		
11	x16 - Device 1 functions 1 and 2 disable (Default Value)	
10	x8, x4 - Device 1 function 1 enable; function 2 disable (Default Value)	
01	Reserved - (Device 1 function 1 disabled; function 2 enable)	
00	x8, x4 - Device 1 function 1 and 2 enable	



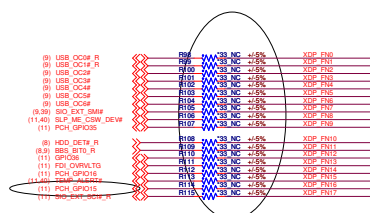
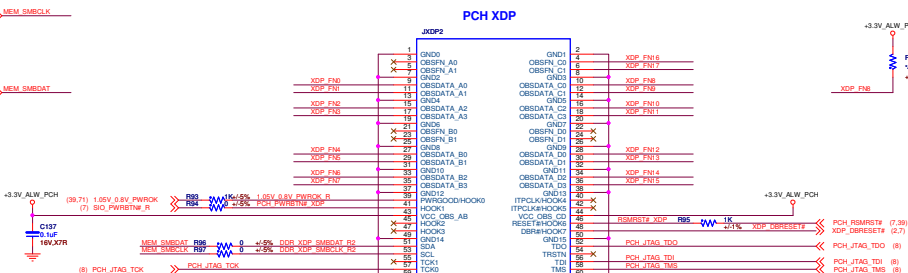


The resistor for R00K2 should be placed such that the stub is very small on CFG0 net



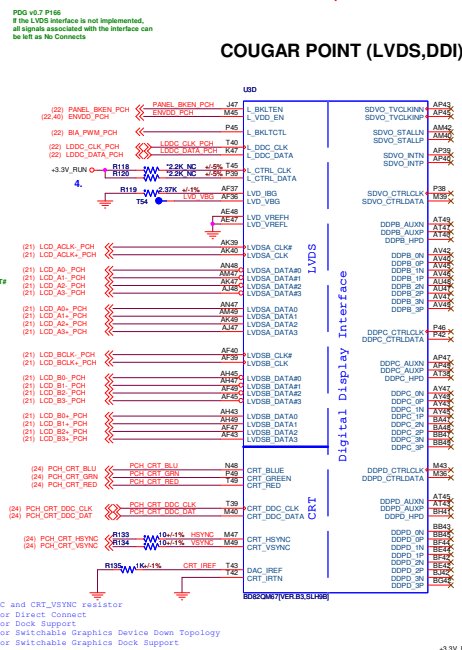
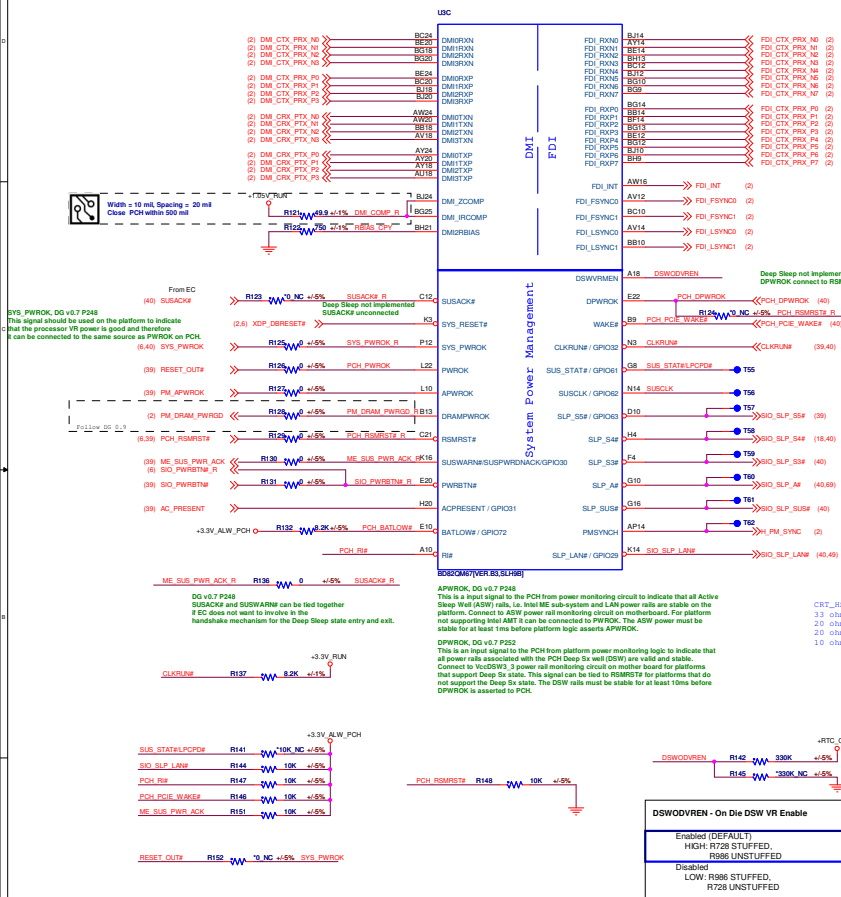
(10,14,15,16,17,18,28,36) MEM\_SMBCLK < MEM\_SMBCLK

(10,14,15,16,17,18,28,36) MEM\_SMBDAT < MEM\_SMBDAT



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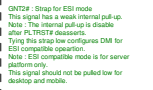
# COUGAR POINT (DMI,FDI,GPIO)





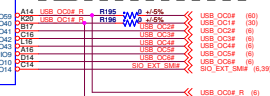
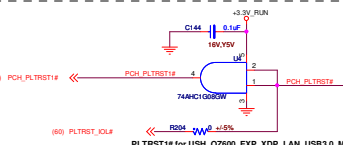
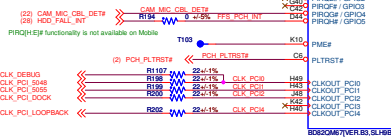
## Cougar Point (PCI,USB,NVRAM)

BBS_BIT[1]	BBS_BIT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

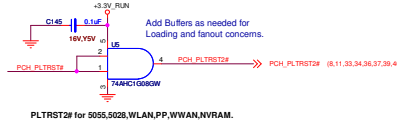
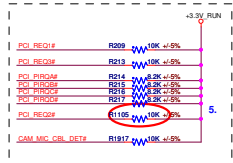
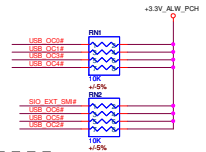


REQ# functionality is not available on Mobile

GNT# functionality is not available on Mobile



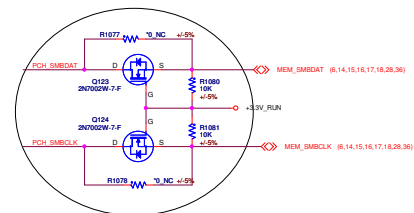
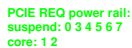
- Right Side pair top
- Right Side pair bottom
- Back Side
- AUX module (Removed)
- 2nd Mini Card (WLAN/WIMAX)
- 1st Mini Card (WWAN)
- 3rd Mini Card
- USH
- DOCK
- DOCK
- Express Card
- BlueTooth
- Camera
- [LCD Touch or Nvidia 3D IR](#)

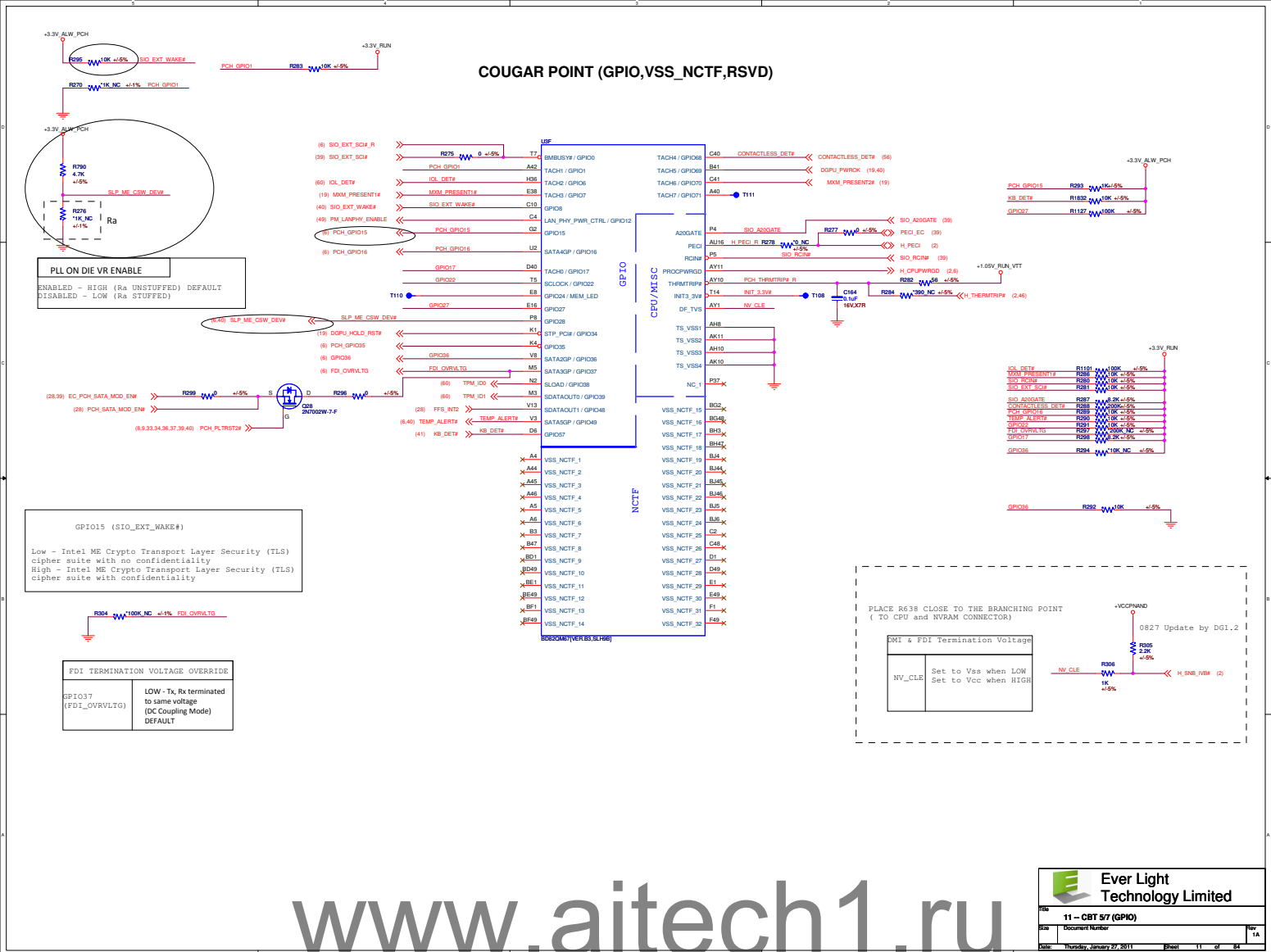


A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low - A16 swap override/Top-Block Swap Override enabled High - Default



1136



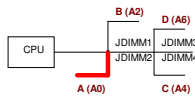






[illegible]

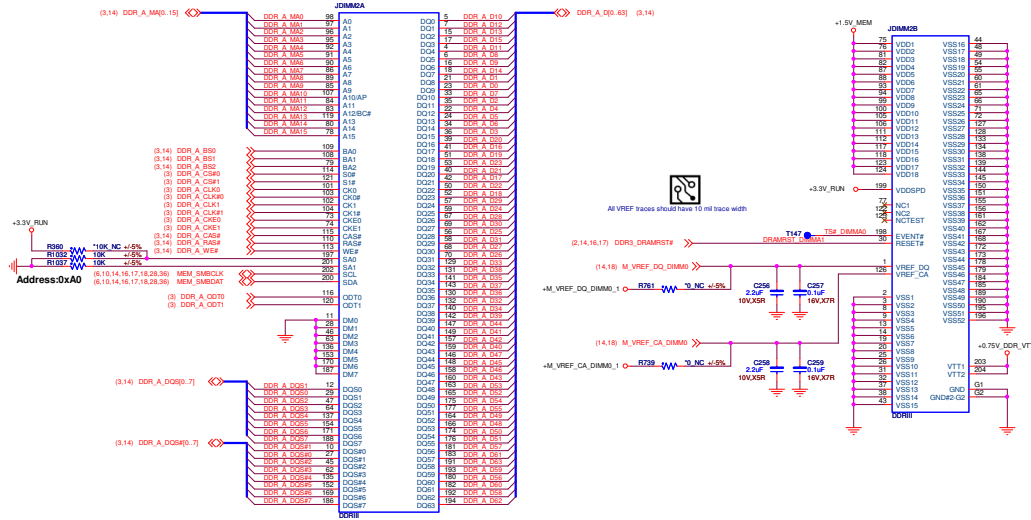




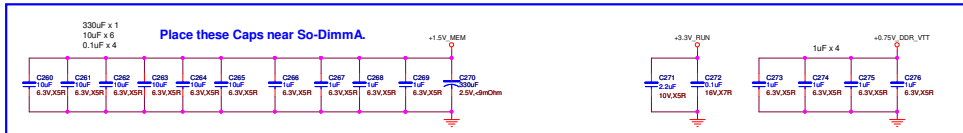
## CHA\_DIMM0\_BOT\_SIDE

JDIMM2 is RVS type.

0510GC: CIS OK



+1.5V S1B5 decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the DIMM. Clock and Control signals. These capacitors should be placed on the same side of the motherboard as the SO-DIMM connector.



DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mls	Strobe + 20 mls

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JDIMM3 is RVS type.  
0526GC: change to RVS type



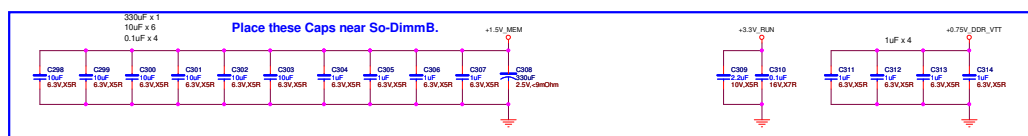
The schematic diagram illustrates a PLL circuit for a 100MHz clock. It includes a 330pF capacitor (C300) and a 100pF capacitor (C301) in series with a 2.5V, 0805 component. The circuit is powered by a 3.3V VDD supply and a 0.75V VDD\_VTT supply. The output of the PLL is connected to a 100MHz clock input. The circuit also includes a 100MHz clock input and a 100MHz clock output. The circuit is powered by a 3.3V VDD supply and a 0.75V VDD\_VTT supply. The output of the PLL is connected to a 100MHz clock input. The circuit also includes a 100MHz clock input and a 100MHz clock output.

Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



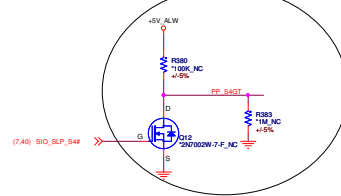
JDIMM4 is STD type.

0510GC: CTS OK

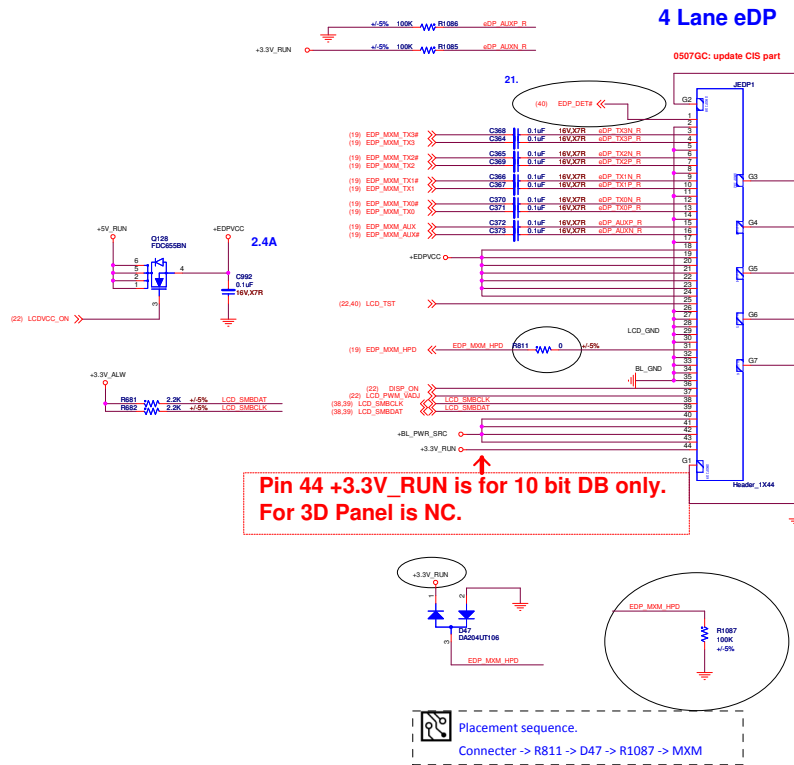


Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils

## M2: Programmable SODIMM VREFDQ



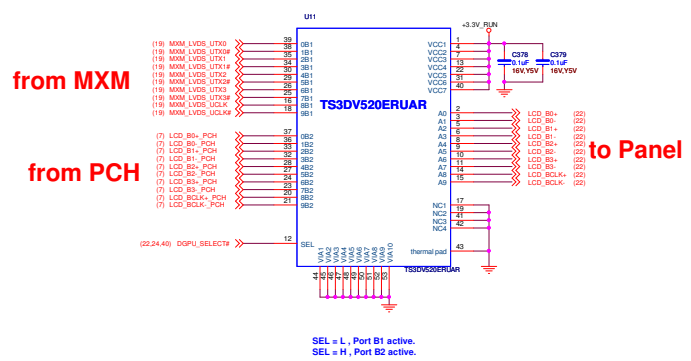
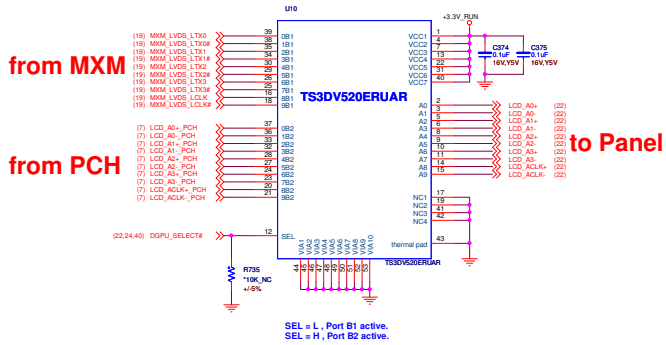




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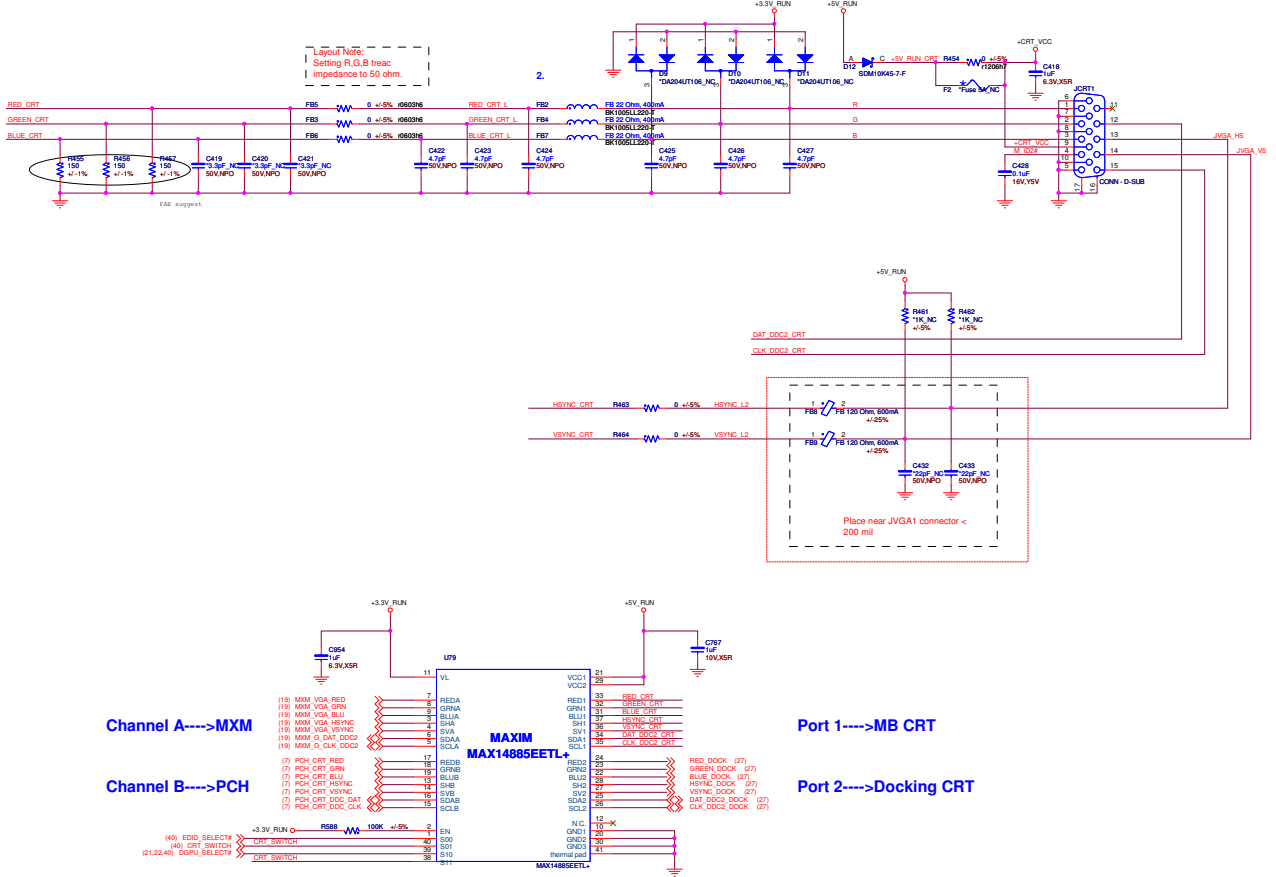
## LVDS MUX for Panel

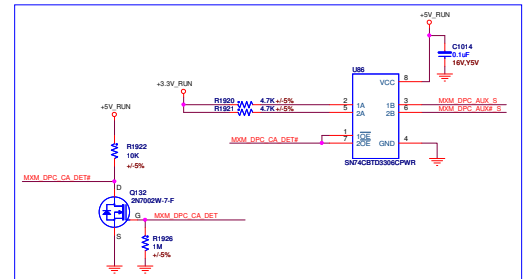
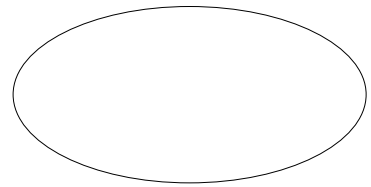


[www.aitech1.ru](http://www.aitech1.ru)

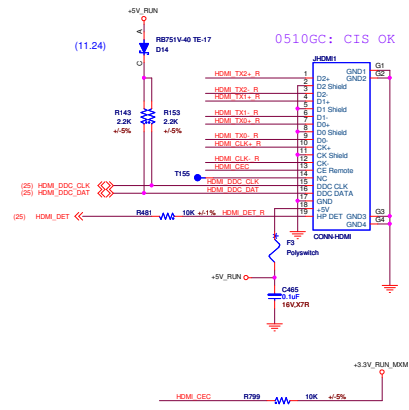
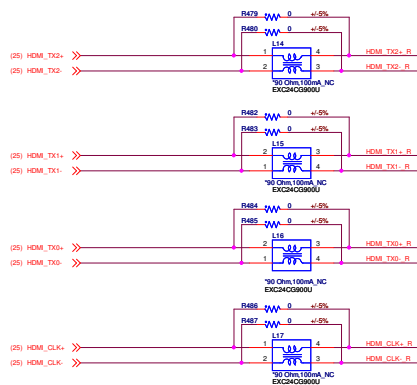
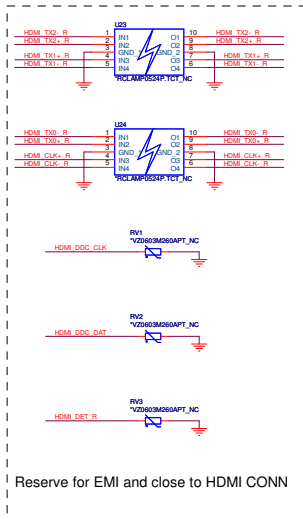






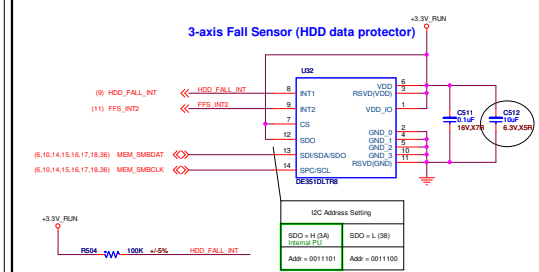
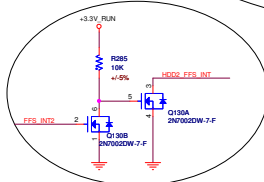
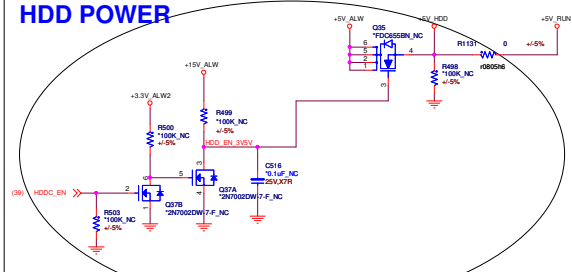


## HDMI CONN

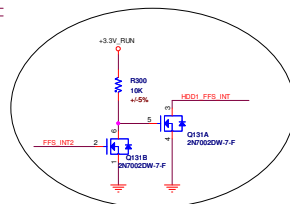




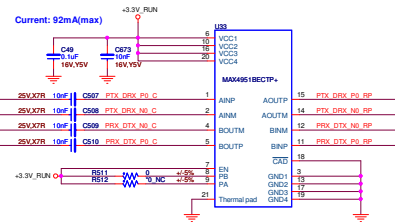
### HDD Connector



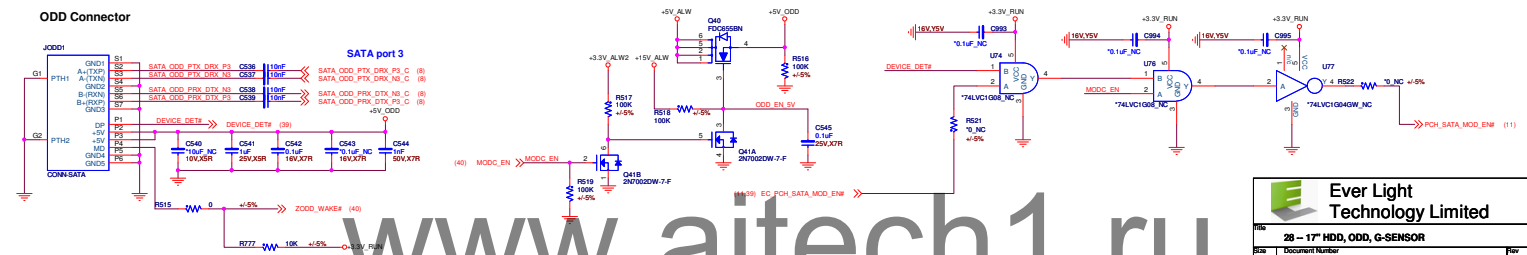
### HDD Connector



Current: 92mA(max)



### ODD Connector



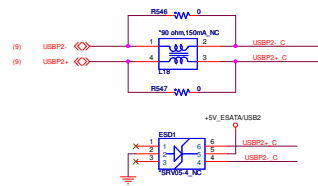
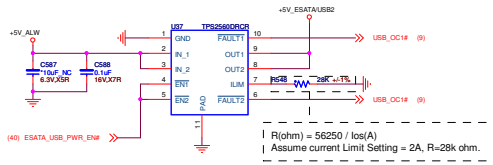
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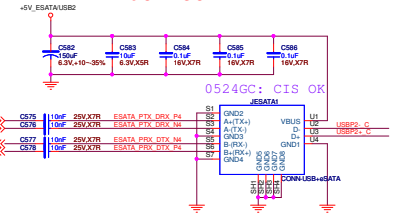
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		Ever Light Technology Limited	
Title		29 - 15" HDD, ODD, G-SENSOR	
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## USB Power

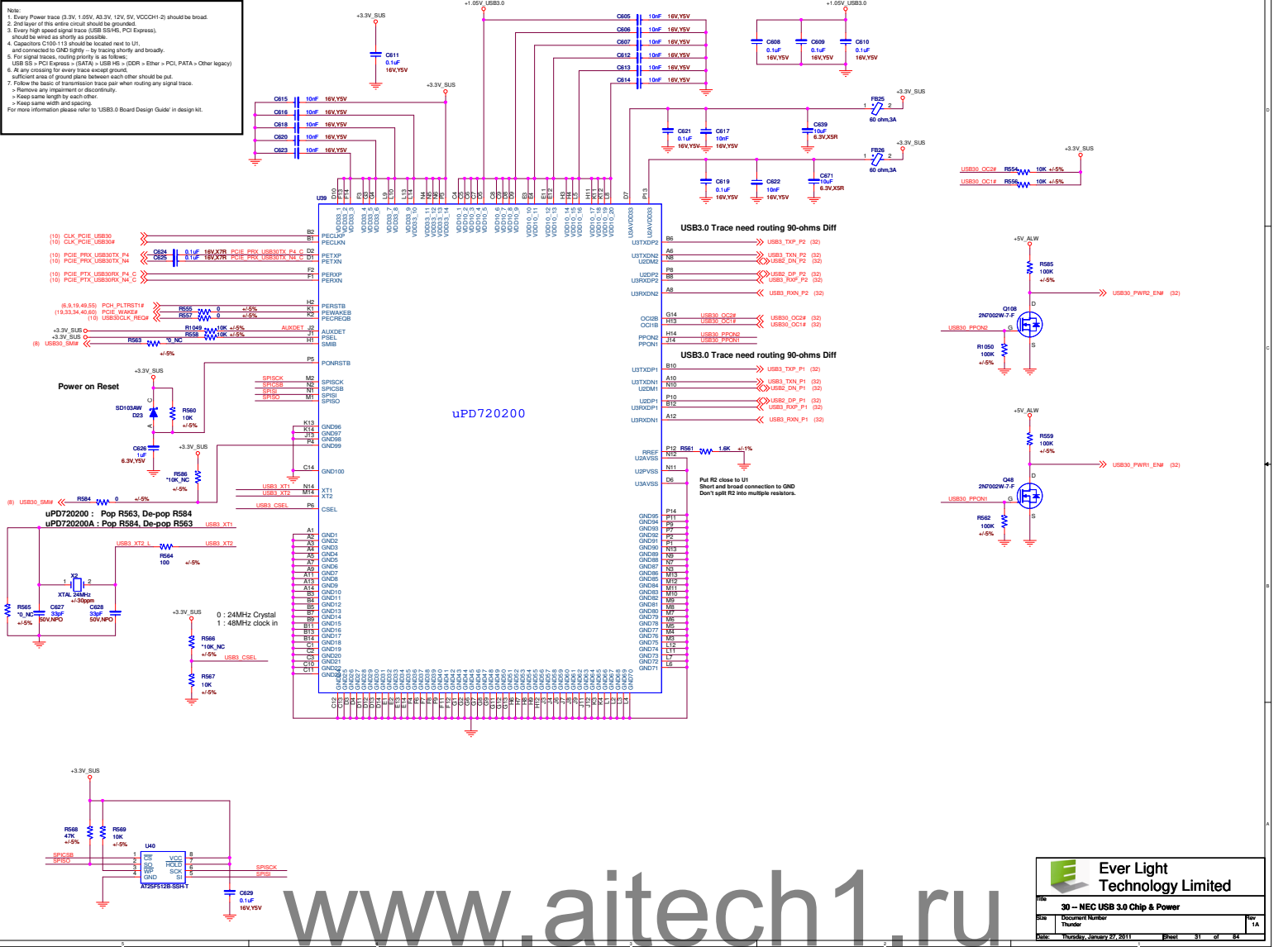


## USB(Back Side) USB+eSATA

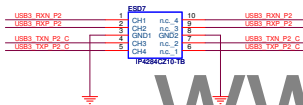
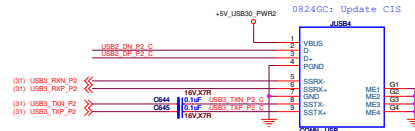
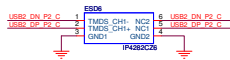
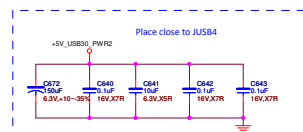
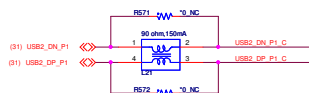
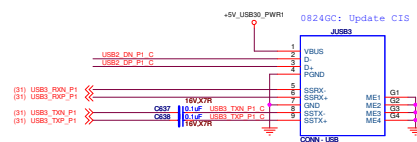
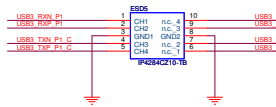
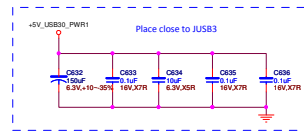
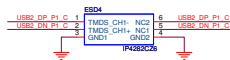
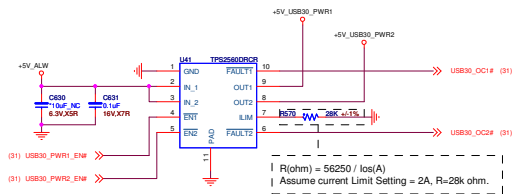


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Note:  
1. Every Power trace (3.3V, 1.05V, A3.3V, 1.2V, 5V, VCCCH1-2) should be broad.  
2. 2nd layer of this entire circuit should be grounded.  
3. Every high speed signal trace (USB, SATA, PCI Express), should be wide as short as possible.  
4. Capacitors C100-113 should be located next to U1, and connected to GND tightly - by tracing shorty and broadly.  
5. For signal traces, routing priority is as follows:  
USB SS > PCI Express > SATA > USB HS > (DDR > Ether > PCI, SATA > Other legacy)  
6. If any crossing for every trace except ground, sufficient area of ground plane between each other should be put.  
7. Follow the basic of transmission trace pair when routing any signal trace.  
8. Remove any impedance or discontinuity.  
9. Keep same length for each other.  
For more information please refer to USB3.0 Board Design Guide in design kit.

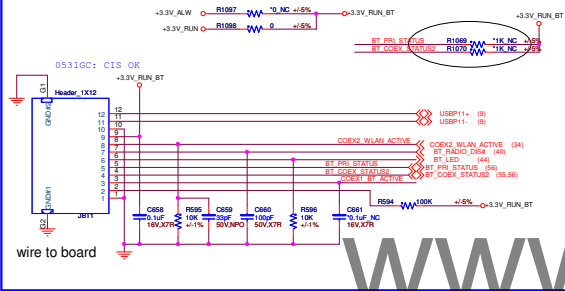
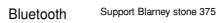
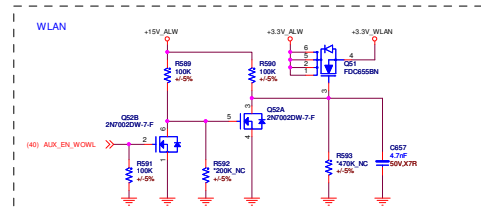
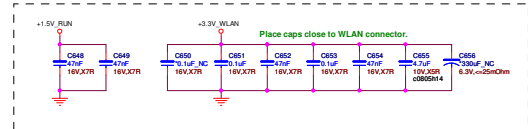
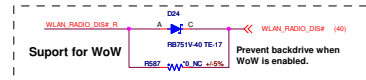
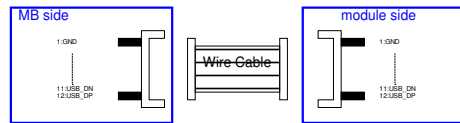
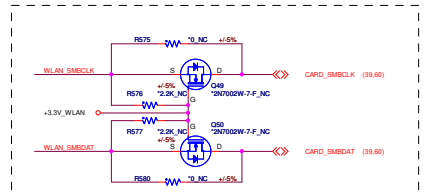


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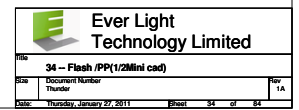


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**2nd MiniCard connector (WLAN, half size)**  
**MiniCard WLAN connector**



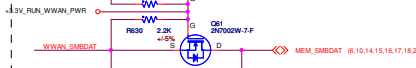
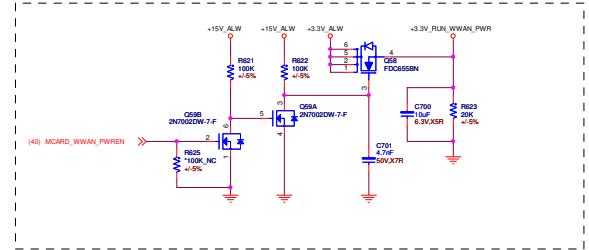
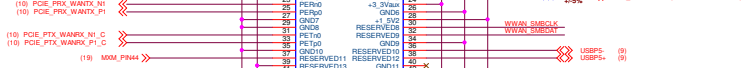
+3.3V\_PP 0510GC: CIS OK



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		Ever Light Technology Limited	
35 - 15" WWMAL SM-AMUX			
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0510GC: CIS OK

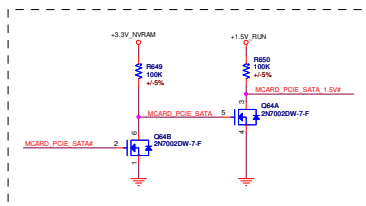
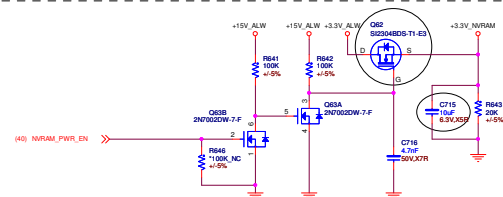
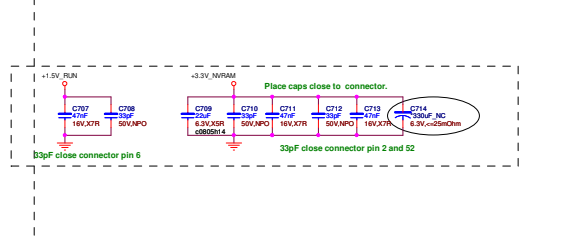


0824GC: update CIS



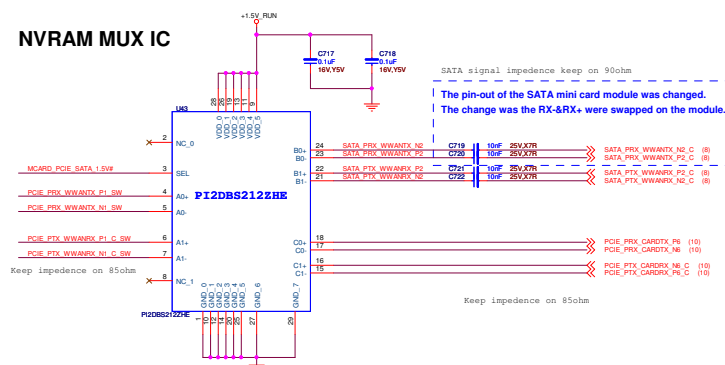


RAM connector  
Full SIZE



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	±0%	1000	750	
	±0%	330	250	250 (wake enable) 5 (S0S wake enable)
+1.5V	±0%	500	375	NA

## NVRAM MUX IC



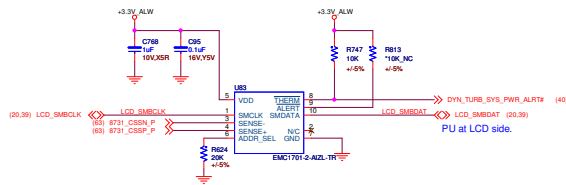
Function	SEL
Port A to Port B	0
Port A to Port C	1

DS\_0412: follow PIG,SATA Port 2


**Ever Light  
Technology Limited**

Title		37 - 17" NVRAM+MUX	
Size	Document Number	Rev	
	Thunder	1/	
Info	Thunder (source) 97 5011	Sheet	97 of 84

# Monitor Charger current

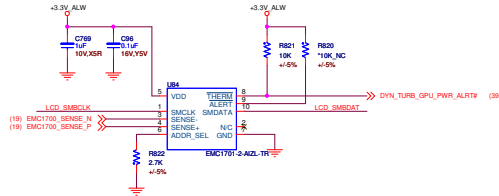


RESISTOR (5%)	SMBUS ADDRESS	RESISTOR (5%)	SMBUS ADDRESS
0	1001_100(r/w)	1600	0101_000(r/w)
100	1001_101(r/w)	2000	0101_001(r/w)
180	1001_110(r/w)	2700	0101_010(r/w)
300	1001_111(r/w)	3600	0101_011(r/w)
430	1001_000(r/w)	5600	0101_100(r/w)
560	1001_001(r/w)	9100	0101_100(r/w)
750	1001_010(r/w)	20000	0101_101(r/w)
1270	1001_011(r/w)	Open	0111_000(r/w)

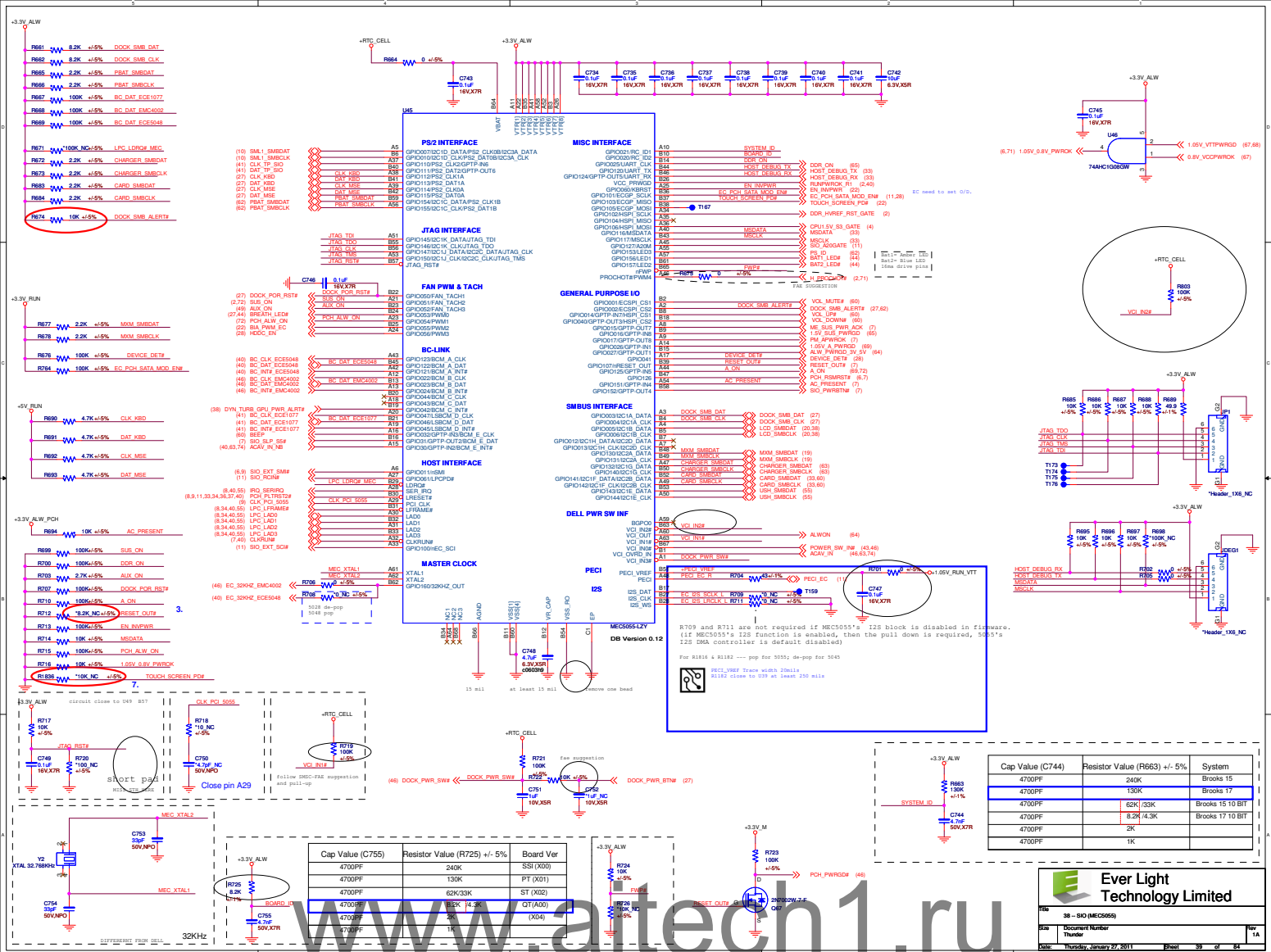
U84

U83

# Monitor PWR\_SRC\_MXM

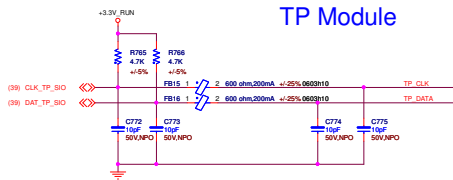


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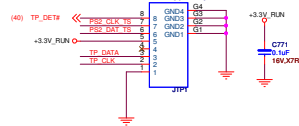




## TP Module

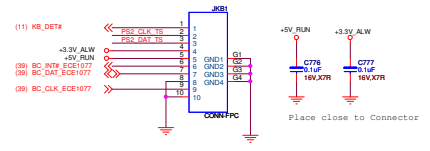


## 0524GC: CIS OK



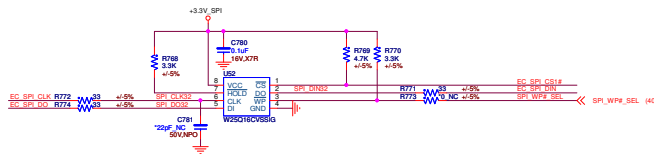
## Keyboard Module

### 1116 update to CIS

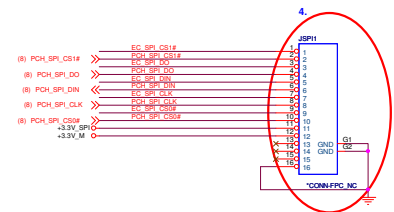
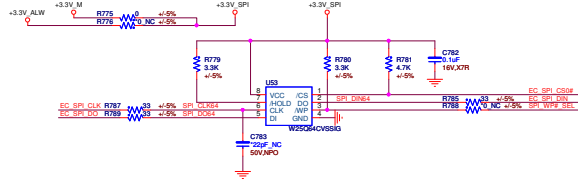


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# PCH, EC SPI ROM For BIOS (2M Byte)



# PCH SPI ROM For IAMT (8M Byte)



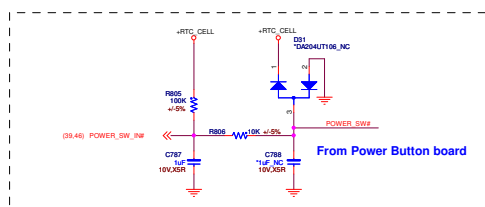
Put close to JSP11

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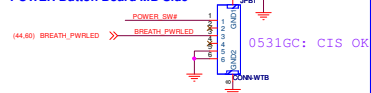
For AUX Module Conn

Remove AUX Module

7.



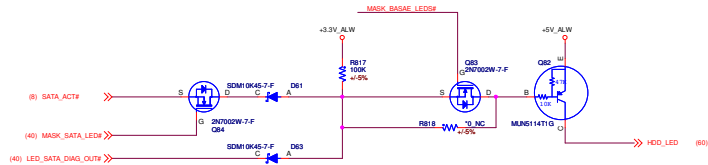
POWER Button Board MB Side



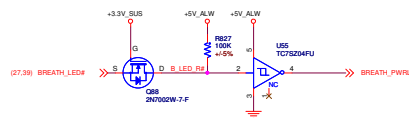
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43 - DB Connector x 7	
Rev	1A
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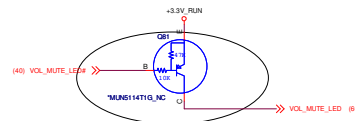
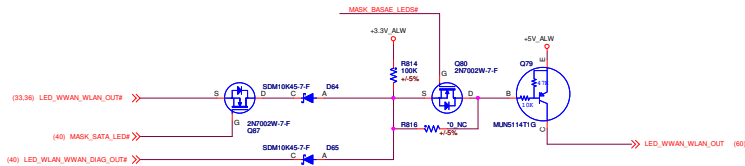
HDD



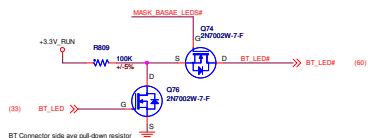
BREATH PWRLED



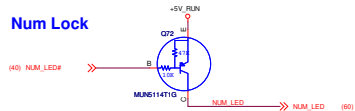
WWAN/WLAN



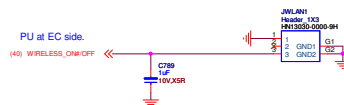
BT



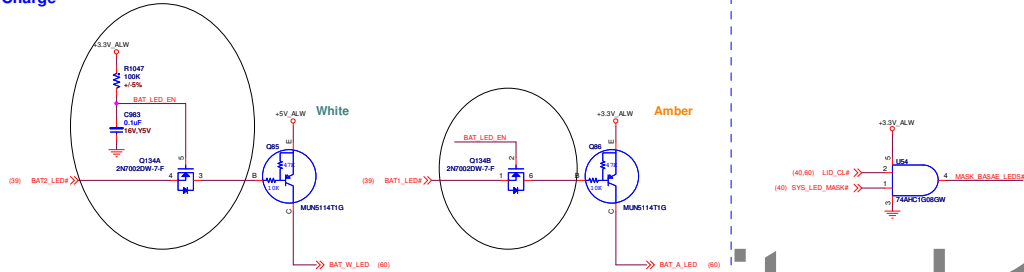
Num Lock



Wireless ON/OFF switch




Charge





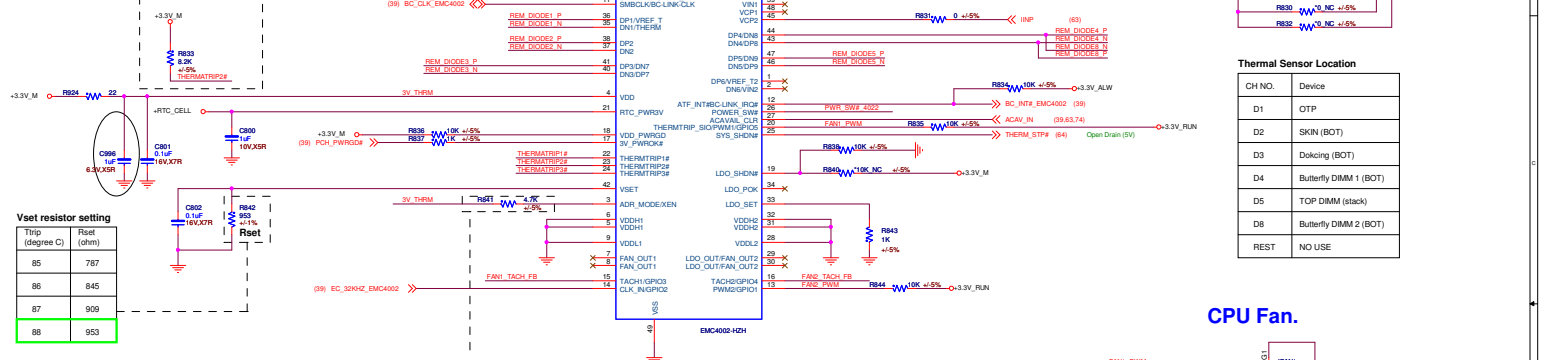
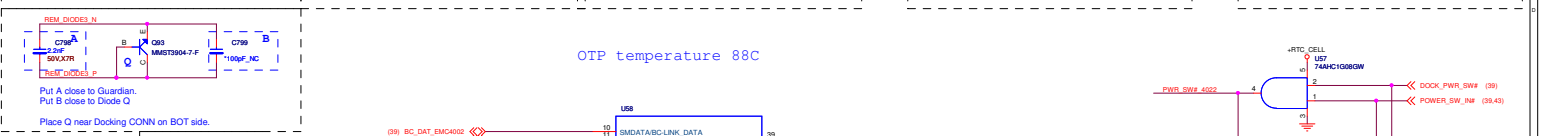
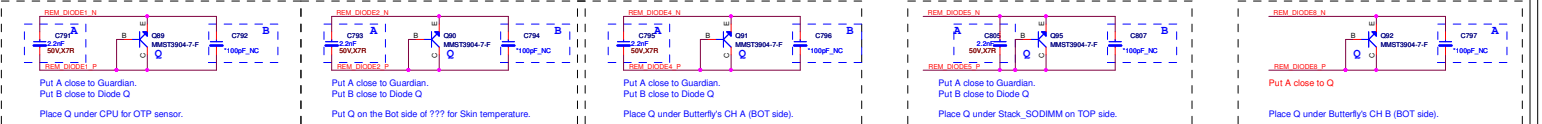
DS\_0412: should be on touch Pad module.

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File		45 - Hall sensor	
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**Vsset resistor setting**

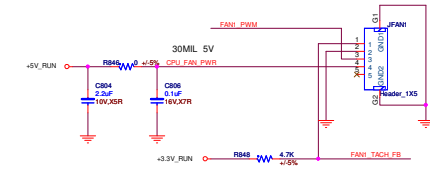
Temp (degree C)	Resist (ohm)
85	787
86	845
87	909
88	953

Pull-up Resistor on ADDR. MODE/XEN	For Remodel mode	SMBUS Address
<=4.7K	2N3904	2F(1w)
10K	2N3904	2E(1w)
18K	Thermistor	2F(1w)
>=33K	Thermistor	2E(1w)

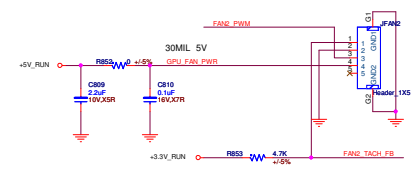
**Thermal Sensor Location**

CH NO.	Device
D1	OTP
D2	SKIN (BOT)
D3	Docking (BOT)
D4	Butterfly DIMM 1 (BOT)
D5	TOP DIMM (black)
D8	Butterfly DIMM 2 (BOT)
REST	NO USE

### CPU Fan.



### GFX Fan



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File: 45 - Thermal 4002 & FAN x 2

Rev: 1A

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		Ever Light Technology Limited	
File 47 - AUDIO(92HD80B)+SPK+JACK			
Rev	Document Number	Rev	1A
Thunder			
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		Ever Light Technology Limited	
48 -- AUDIO for Docking+Crystal			
Rev	Document Number	Rev	1A
Thunder			
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		Ever Light Technology Limited	
File: 50 - TPM for China			
Rev	Document Number	Rev	1A
	Thunder		
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		Ever Light Technology Limited	
File S1 - Card Reader & Conn			
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	Thunder		
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		Ever Light Technology Limited	
File 52 - 15" 1394 Conn			
Rev	Document Number	Rev	1A
	42600		
Date: Thursday, January 27, 2011		Sheet	55 of 84

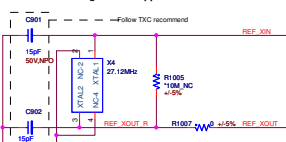
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		Ever Light Technology Limited	
File: 53 - 17" 1394 Conn+ Power			
Rev	Document Number	Rev	1A
	Thunder		
Date: Thursday, January 27, 2011		Sheet	55 of 85

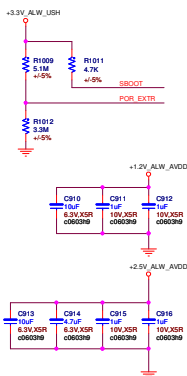


JTAG\_TDI\_USH R994 10M  $\pm 5\%$  JTAG\_CLK\_USH  
 JTAG\_TMS\_USH R995 10M  $\pm 5\%$  JTAG\_TDO\_USH  
 JTAG\_USH R996 10M  $\pm 5\%$  JTAG\_RSTN\_USH  
 HF\_RX\_TEST1 R997 10M  $\pm 5\%$  HF\_RX\_TEST2  
 HF\_RX\_TEST3 R998 10M  $\pm 5\%$  HF\_RX\_TEST2

27.12MHz regardless support RFID or not.

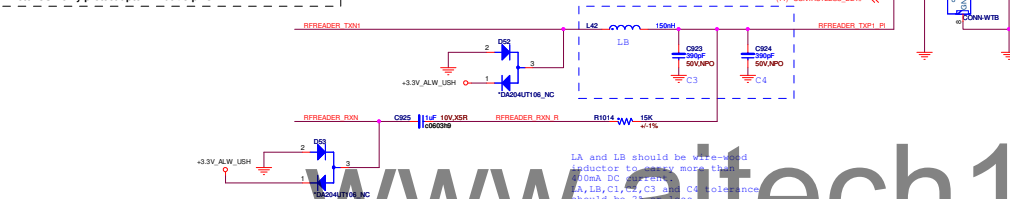


\* XTAL CIRCUIT (COMPONENTS + WIRING) SHOULD BE ON TOP LAYER ONLY, TO CONTROL INTERFERENCE

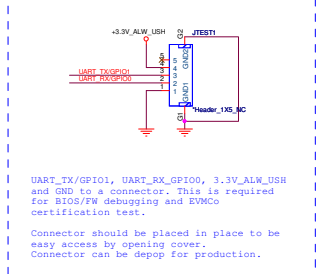
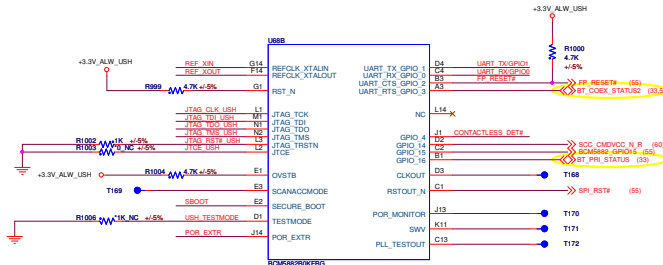


BRGM - D87, D88, D89, D90 are required for ESD protection, but they could be removed if ODM can guarantee 8kV protection to USH after contacted ESD test.

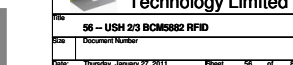
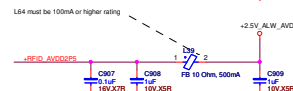
Note: USH only protect upto 2kV at I/O pins.



LA and LB should be wire-wound inductor to carry more than 100mA DC current. Inductance of LA and LB should be 25uH or less.




UART\_TX/GPIO1, UART\_RX/GPIO0, 3.3V\_ALW\_USH and GND to a connector. This is required for BIOS/FW debugging and EVMCo certification test.  
 Connector should be placed in place to be easy access by opening cover.  
 Connector can be depop for production.

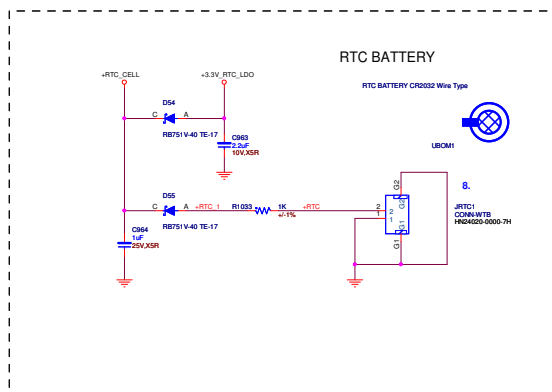


Ever Light Technology Limited	
File	56 - USH 23 BCM5882 RFID
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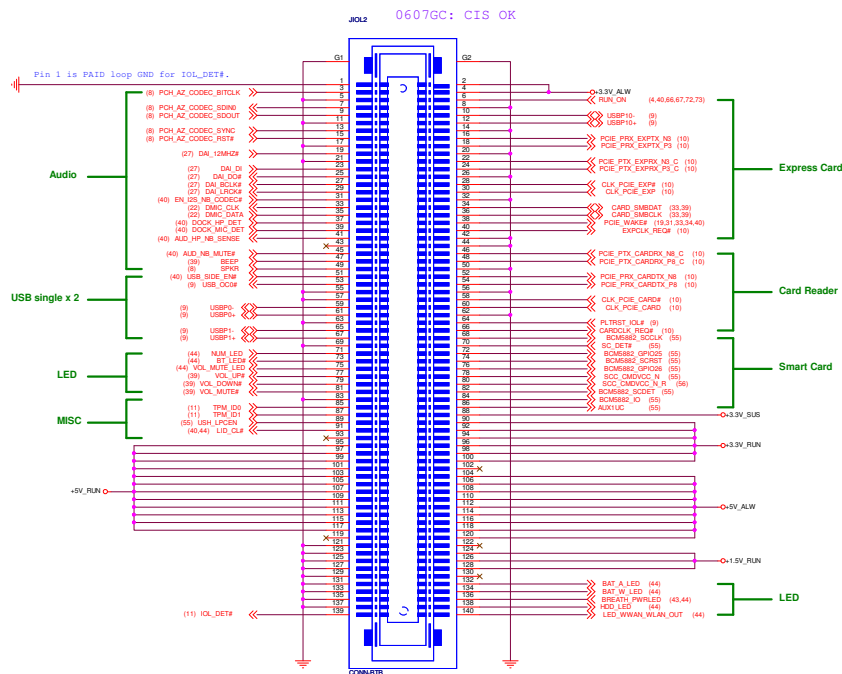
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		Ever Light Technology Limited	
File: S8 -- Smart Card IC & Conn			
Rev: Document Number		Rev: 1A	
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 <b>Ever Light Technology Limited</b>	
<b>S0 - System Reset, RTC</b>	
Rev Document Number Thunder	Rev 1A
Date: Thursday, January 27, 2011      Sheet: 55 of 84	

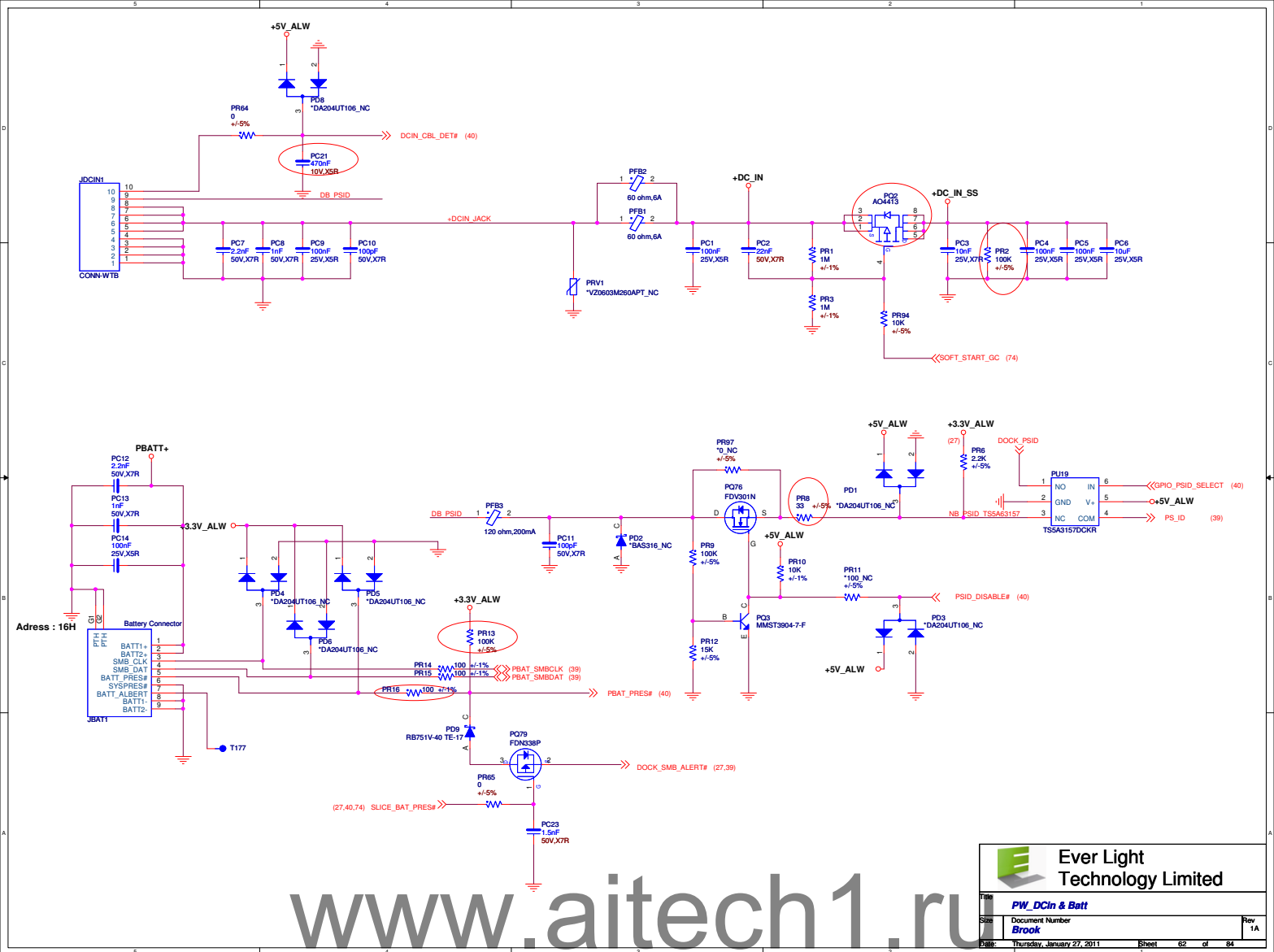


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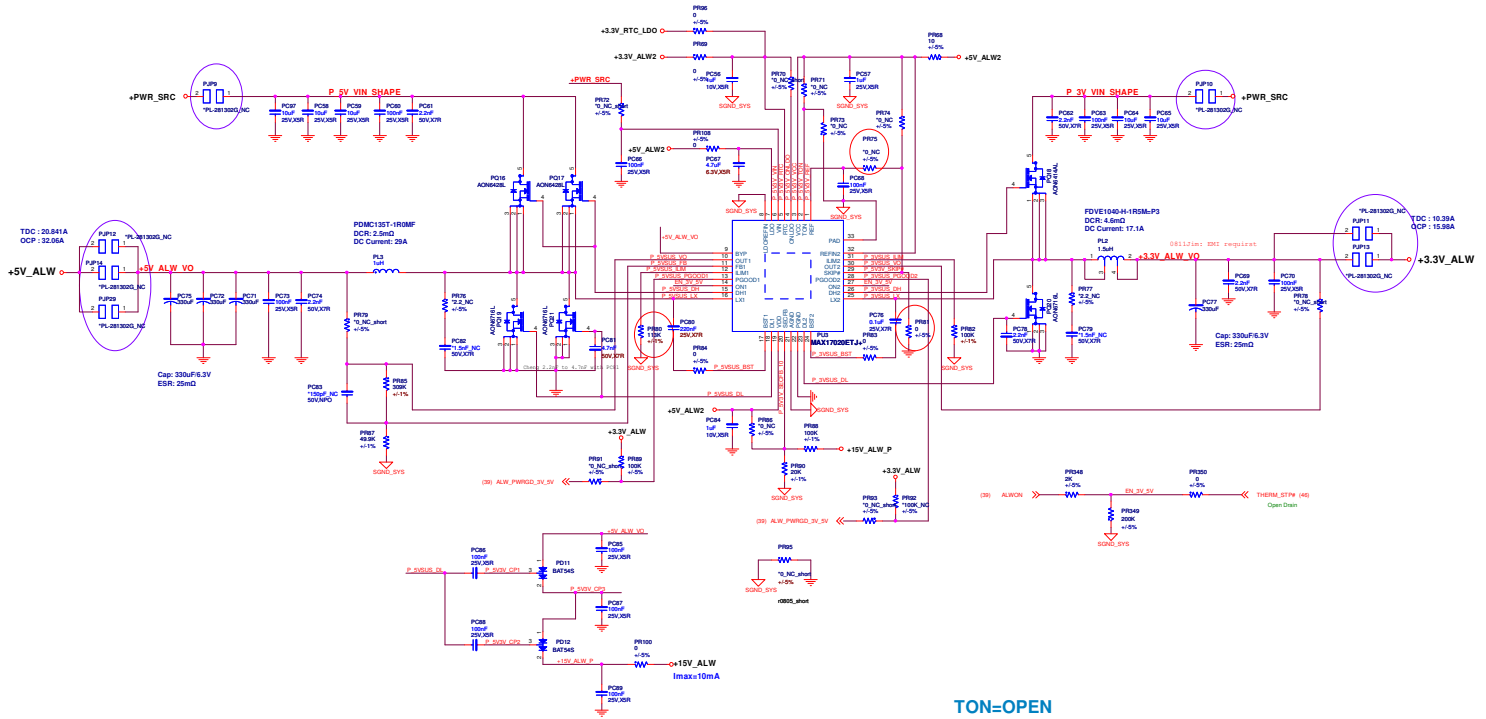
		Ever Light Technology Limited	
Title 78 - Blank Page			
Rev	Document Number		Rev 1A
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## +5V\_ALW / +3.3V\_ALW POWER SUPPLY



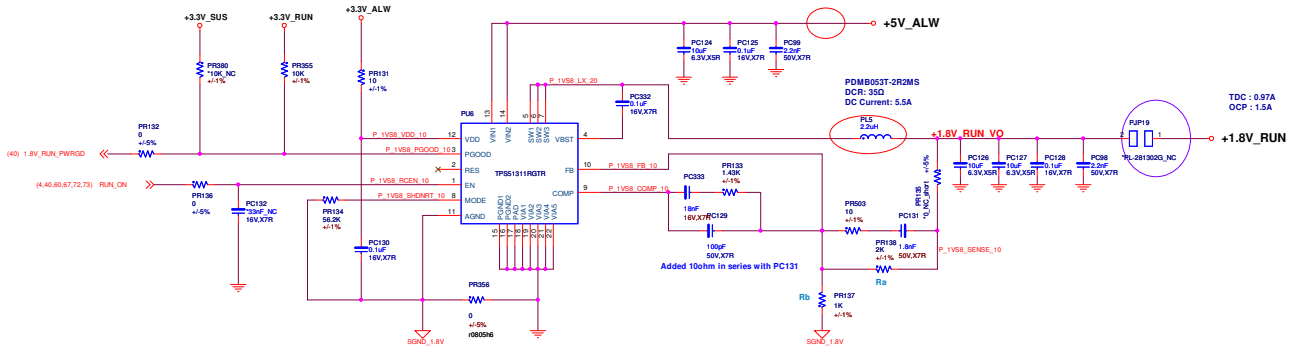
TON=OPEN  
5V:Fsw=400KHZ  
3V:Fsw=300KHZ  
SKIP#=VCC=>Forced-PWM mode  
SKIP#=REF=>Ultrasonic mode  
SKIP#=GND=>Pulse-skipping mode



VDDQ_CTRL01	VDDQ_CTRL00	+1.5V_MEM
HIGH	HIGH	1.513V
HIGH	LOW	1.561V
LOW	HIGH	1.601V
LOW	LOW	1.655V

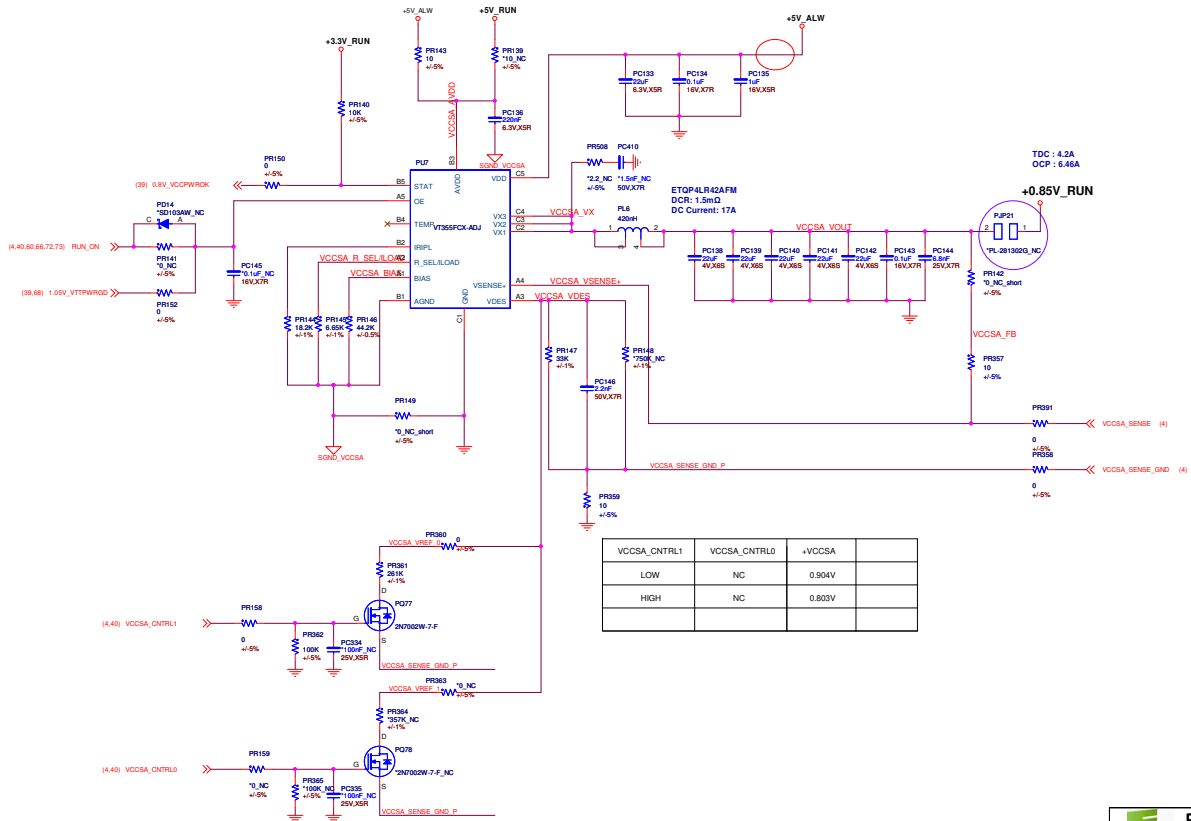
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## +1.8V\_RUN POWER SUPPLY



Variant Name:	
Ever Light Technology Limited	
PW_SW_+1.8V(TPS51311)	
Rev	1.0
Docu Number	Brooks
Date	Thursday, January 29, 2011
Sheet	18 of 54

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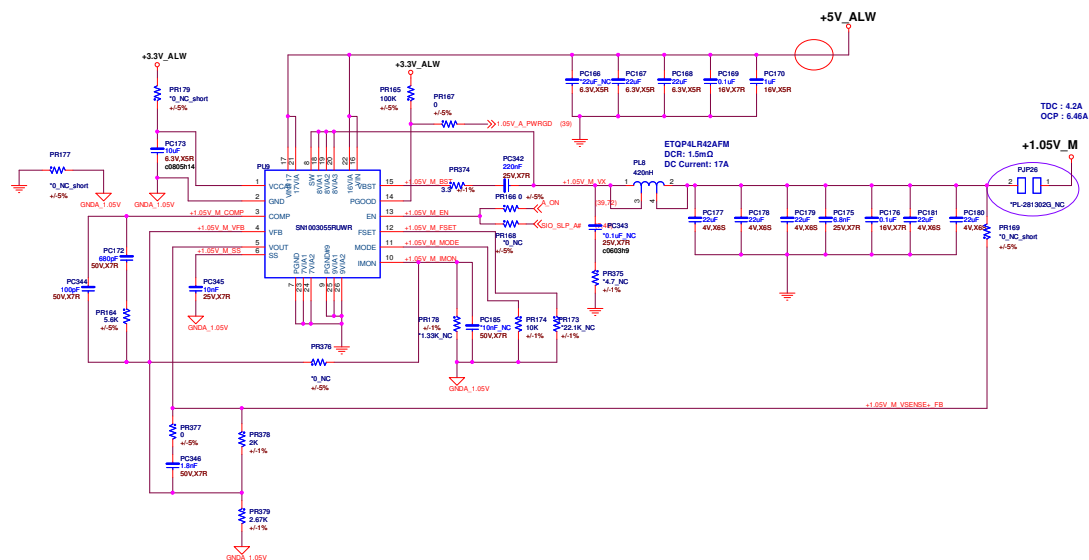


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File	PW_+1.05VM(V7355)	
Rev	Document Number	Rev
Brooks		1A
Date	Thursday, January 27, 2011	Sheet 03 of 04

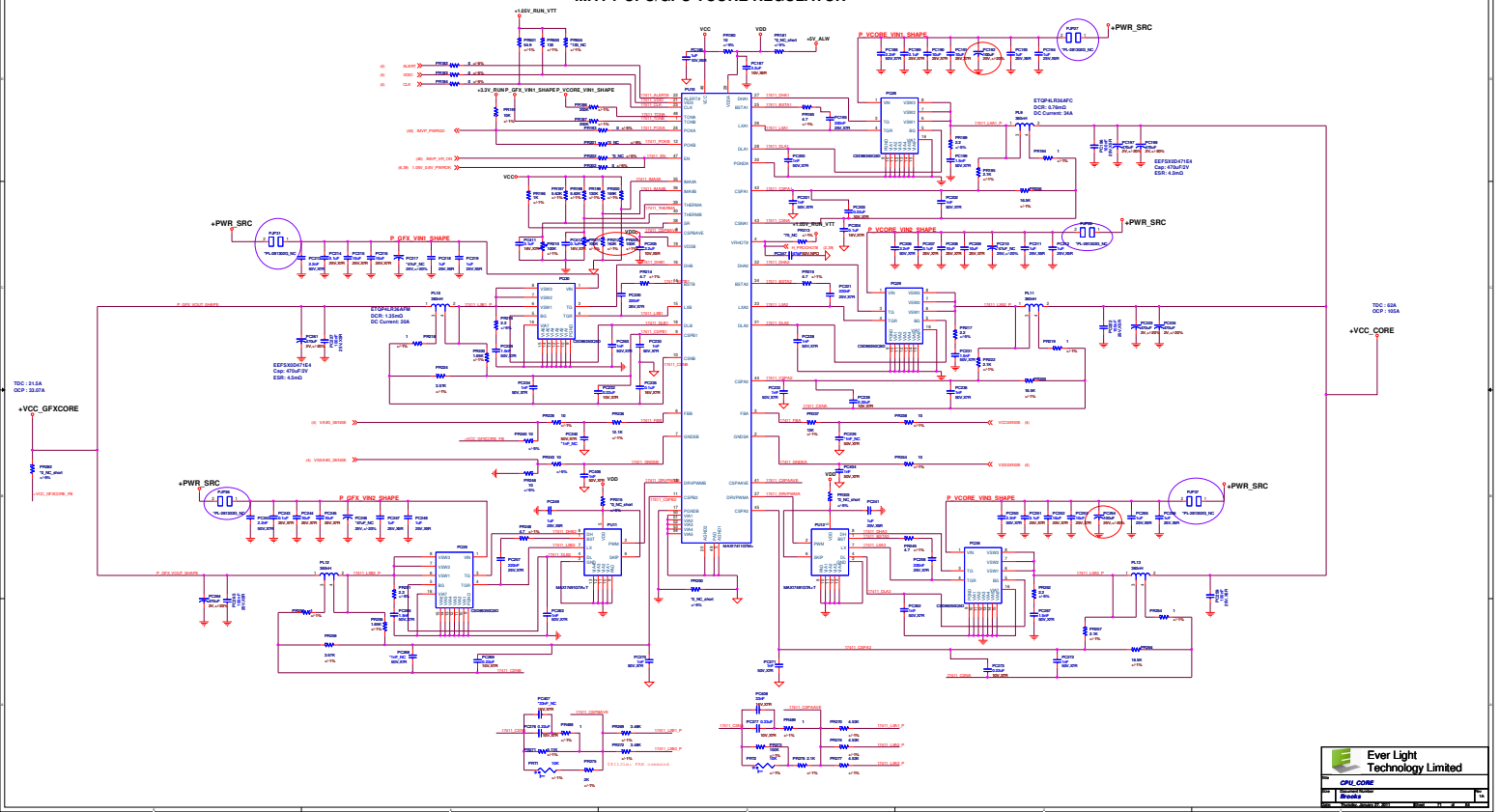
www.aitech1.ru

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

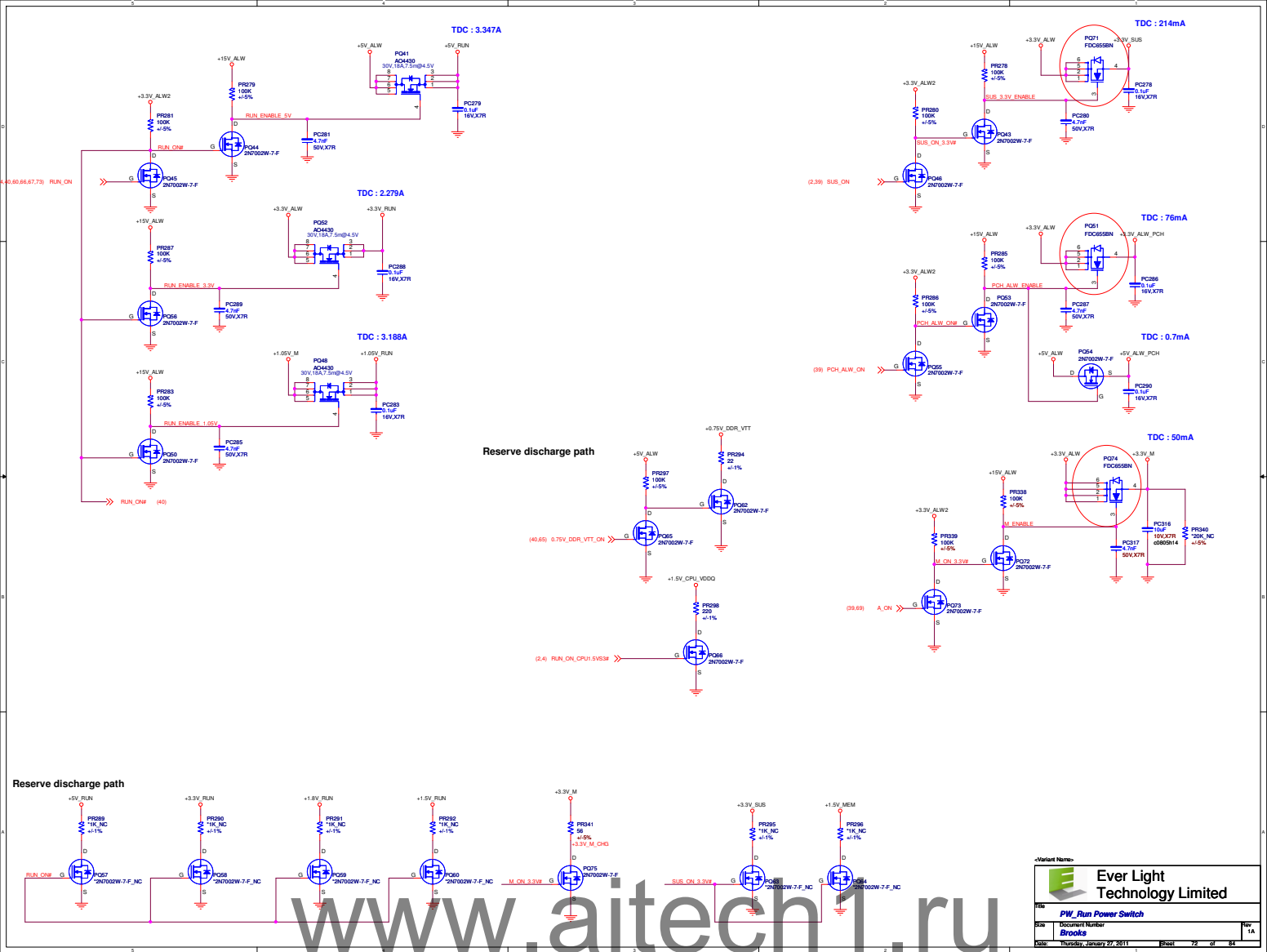
www.aitech1.ru

Title			<Title>		
Size	Document Number		Rev	<Rev Co	
A	<Doc>		<Doc>	<Rev Co	
Date:	Thursday, January 27, 2011		Sheet	70	of 84

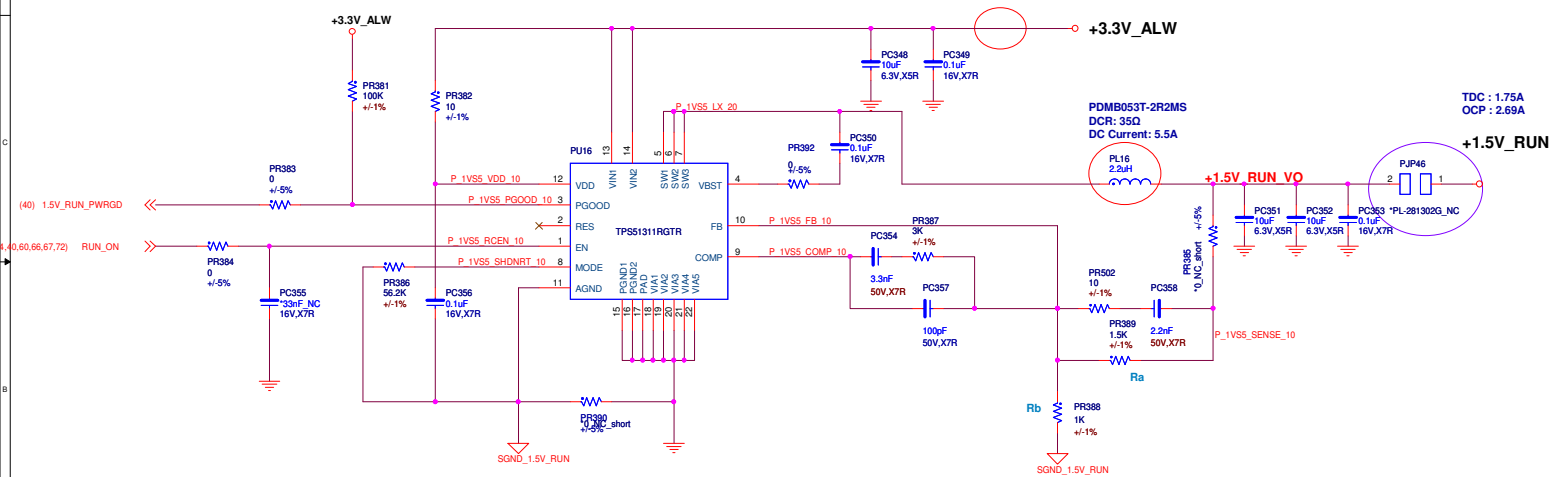
# IMVP7 CPU/GPU VCORE REGULATOR



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## +1.5V\_RUN POWER SUPPLY



<Variant Name>



Ever Light  
Technology Limited

File **PW\_SW\_+1.8V(TPS51311)**


Size **Brooks**

Date: Thursday, January 27, 2011

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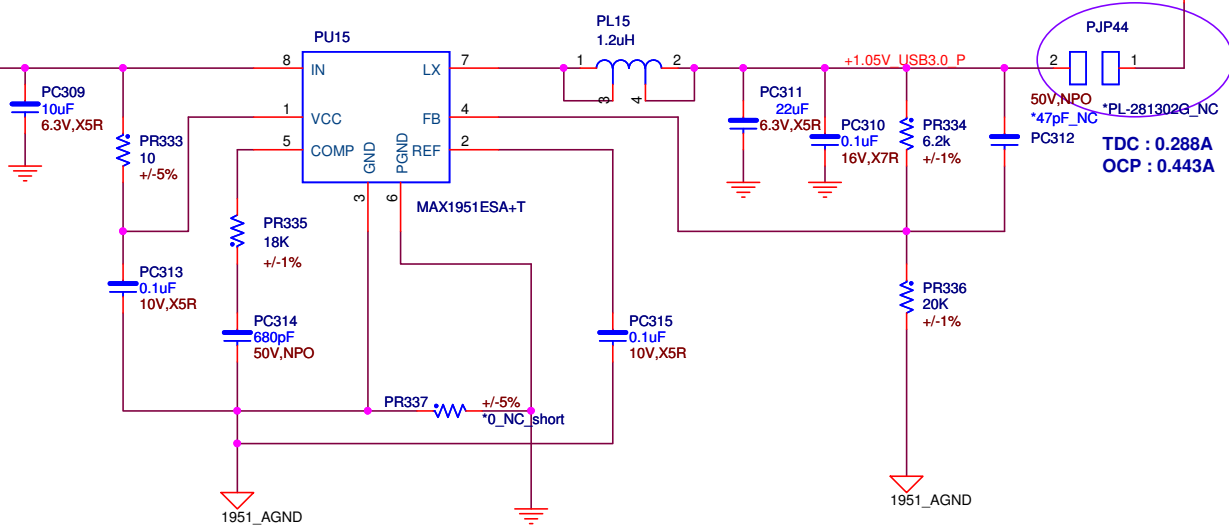


		<b>Ever Light Technology Limited</b>	
<b>+12V_1394(MAX688)</b>			
File	Document Number		Rev
Size	<b>Brooks</b>		1A
Date:	Thursday, January 27, 2011	Sheet	75 of 84

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+3.3V\_SUS

+1.05V\_USB3.0

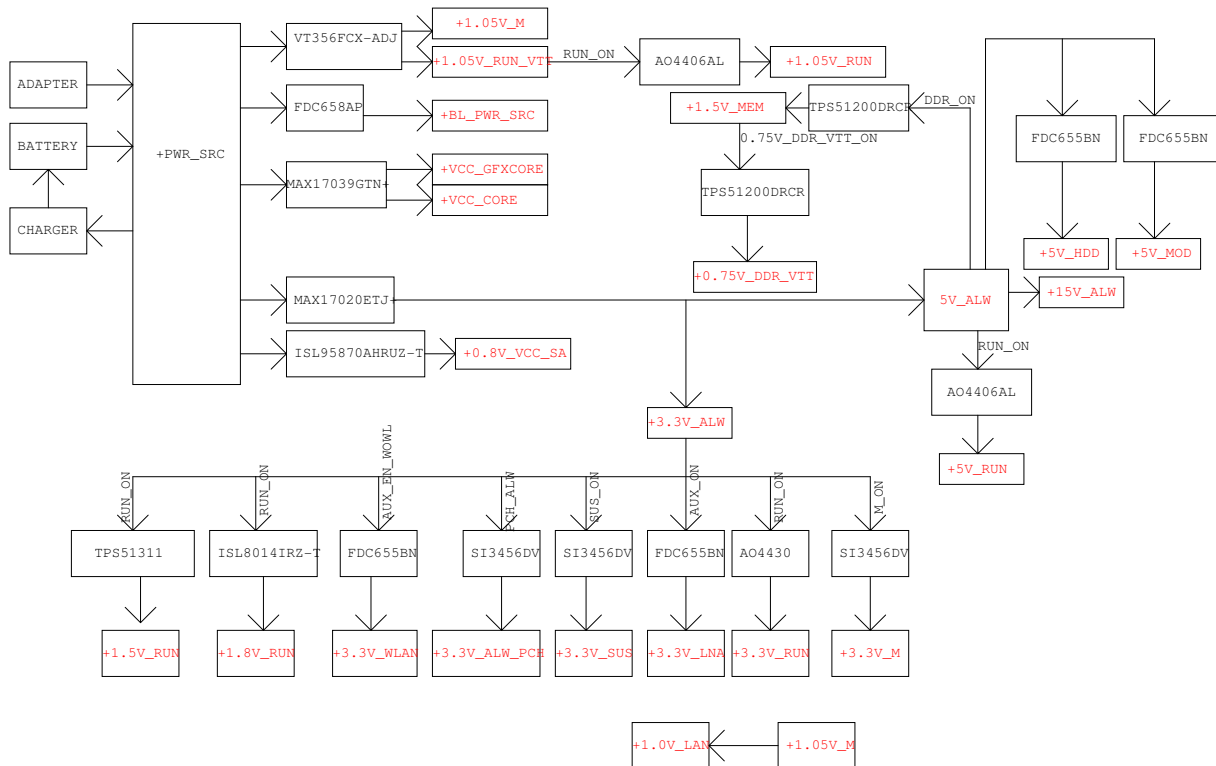


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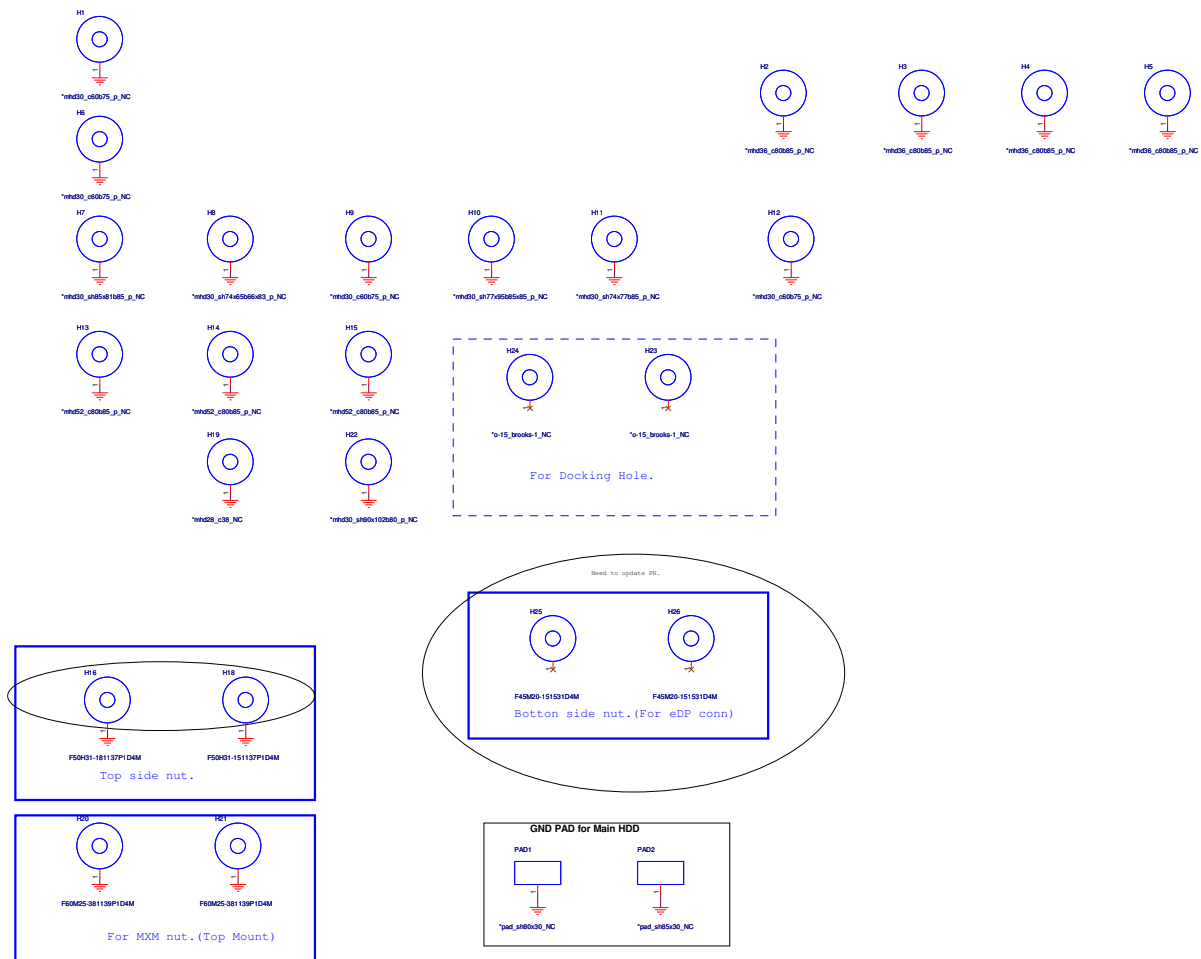
Title			
+1.05V_USB3.0			
Size	Document Number		Rev
	Brooks		1A
Date:	Thursday, January 27, 2011		Sheet 76 of 84

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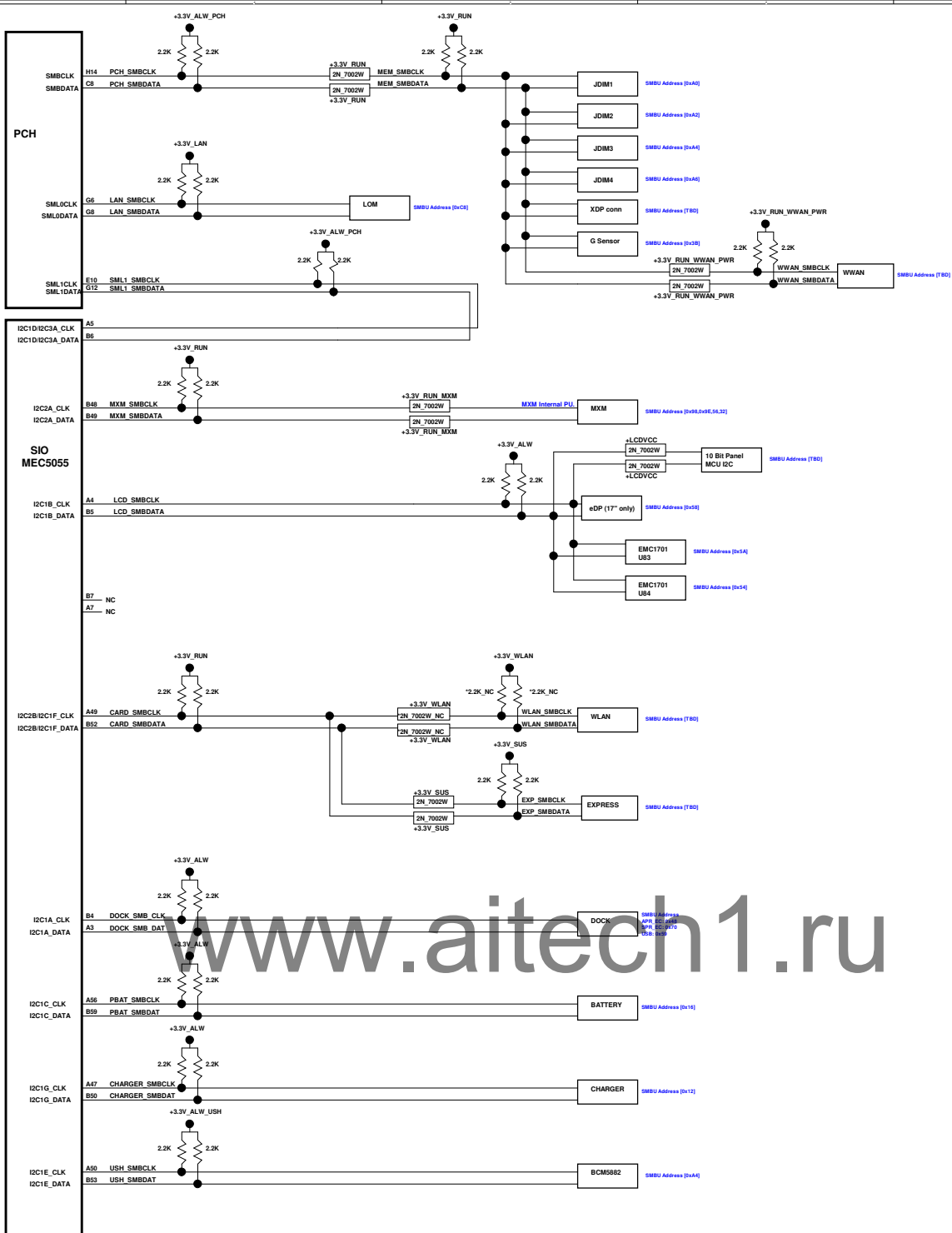





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		Ever Light Technology Limited	
File		73 - Power Sequence Diagram	
Rev	Document Number	Rev	
	Thunder	1A	
Date		Thursday, January 27, 2011	Sheet 05 of 05

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		Ever Light Technology Limited	
Title			
74 – Power Sequence Timing			
Size		Rev	
Document Number Thunder		1A	
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to HDD) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (Soft off) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	ON	ON	OFF	OFF
S4 (Suspend to HDD) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (Soft off) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ Power Plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	Right Side top
	1	Right Side bot
	2	Back Side
	3	NC
	4	2nd Mini Card (WLAN/WIMAX)
	5	1st Mini Card (WWAN)
	6	3rd Mini Card
	7	USH
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	BlueTooth
	12	Camera
	13	LCD Touch or Nvidia 3D IR
USH	0	BTO
	1	NC

PCH	PCI EXPRESS	DESTINATION
	Lane 1	1st Mini Card WWAN
	Lane 2	2nd Mini Card WLAN
	Lane 3	Express Card
	Lane 4	USB 3.0
	Lane 5	3rd Mini-Card
	Lane 6	4th Mini-Card
	Lane 7	LAN
	Lane 8	Card Reader

PCH	SATA	DESTINATION
	SATA 0	HDD 1st
	SATA 1	HDD 2nd
	SATA 2	MINI CARD
	SATA 3	ODD
	SATA 4	E-SATA
	SATA 5	Docking

MXM Graphics Module	MXM PORT	CONNECTION
	PORT A	MB DP Port
	PORT B	DOCK DP2
	PORT C	DOCK DP1 and MB HDMI
	PORT D	eDP Panel

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